Atomic layer deposited zinc tin oxide channel for amorphous oxide thin film transistors

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Bottom-gate thin film transistors with amorphous zinc tin oxide channels were grown by atomic layer deposition. The films maintained their amorphous character up to temperatures over 500 °C. The highest field effect mobility was ∼13 cm^2/V·s with on-to-off ratios of drain current ∼10^9–10^{10}. The lowest subthreshold swing of 0.27 V/decade was observed with thermal oxide as a gate insulator. The channel layers grown at 170 °C showed better transistor properties than those grown at 120 °C. Channels with higher zinc to tin ratio (∼3–4) also performed better than ones with lower ratios (∼1–3). © *2012 American Institute of Physics*. [http://dx.doi.org/10.1063/1.4752727]

Amorphous metal oxide semiconductors have been extensively studied over the past ten years as promising channel materials for thin film transistors (TFTs), organic light-emitting diodes (OLEDs) and liquid crystal displays (LCDs).[1–3] The large demand for low power consumption with better performance of such devices requires a new semiconductor material exhibiting better transistor properties, i.e., higher mobility, smaller subthreshold swing (SS) and higher ratio of on-to-off drain current (I_{ON}/I_{OFF}). The demonstration of amorphous indium gallium zinc oxide (a-IGZO) transistors by Nomura *et al*., drew huge attention to ZnO-based materials.[4] It showed a large mobility of 6–9 cm^2/V·s with good stability. Their amorphous nature enables excellent stability and uniformity over large area devices unlike poly-silicon-based devices. Zinc tin oxide (ZTO) is one of the ZnO-based oxides which has been highlighted recently due to its high stability with reasonable mobility up to 15 cm^2/V·s.[5] Also, ZTO does not contain indium or gallium, so it is free of toxic, expensive and scarce elements.

Generally, sputtering has been used for the growth of ZTO channel layers with its easy control on carrier concentrations by adjusting operating conditions.[5–9] Other growth methods, such as pulsed laser deposition,[10] solution deposition,[11] inkjet printing[12] and combustion[13] have been reported. However, growth of ZTO by atomic layer deposition (ALD) and detailed study of its performance in devices have remained largely unexplored up to now. Growth with exceptional controllability over elemental composition and thickness is one of the advantages of ALD.[14] Uniform composition and thickness are also maintained in ALD films over rough surfaces and inside narrow holes, which conventional sputtering cannot provide easily for possible three-dimensional device structures. ALD offers the possibility of selective deposition only on some areas while avoiding deposition on other areas that are deactivated, for example, by imprint lithography.[15,16] Thus films can be patterned without any etching step. This patterning process is superior to conventional etching or lift-off in that no coating material is wasted, and no toxic liquid waste (etchant or photo-resist solvent) is created. In addition, ALD is suitable for deposition on the increasingly large display panels planned for the next generation. In order to achieve these highly desirable properties for ALD of multicomponent amorphous oxides, the ALD temperature windows of the different components must overlap. For example, diethylzinc, the most popular zinc precursor in ZnO-ALD, exhibits an ALD window from roughly 120 to 170 °C. Therefore, an ALD process for SnO_2 showing an overlapping ALD temperature window should be used to realize ideal ALD of ZTO. Recently the authors have demonstrated low-temperature (60–250 °C) ALD of tin dioxide (SnO_2) using a cyclic amide of Sn(II) (1,3-bis(1,1-dimethylethyl)-4,5-dimethyl-(4R,5R)-1,3,2-diazastannolidin-2-ylidene) as the tin precursor.[17] By combining well-established ZnO ALD with this SnO_2 process, fabrication of ZTO-based transistors with good properties is demonstrated in this letter.

Diethylzinc (Sigma Aldrich) and a cyclic amide of Sn(II) were used as the zinc and tin precursors, respectively. As a common oxidant, 50 wt. % hydrogen peroxide (H_2O_2, Sigma Aldrich) was used. ALD-SnO_2 growth behavior with the Sn(II) precursor is reported elsewhere.[17–19] Instead of a stop-flow ALD injection scheme,[20] a conventional constant flow scheme was employed in this study to obtain a more uniform tin concentration profile along the long substrate holder (∼30 cm). The observed saturation growth rate was ∼1.2–1.3 Å/cycle. Although its growth rate was somewhat lower than that from the stop-flow scheme, similar electrical properties were obtained. Growth temperature was mainly 170 °C, which is the upper-bound temperature for ZTO ALD. The ZTO growth was done by repeating a supercycle, x-times subcycle of ZnO (diethyl zinc/purge/H_2O_2/purge) followed by y-times subcycle of SnO_2 (Sn precursor/purge/H_2O_2/purge). Purge time was set to be 30 s. Following a notation of xZyT is preferred here. For example, 3Z1T means 3 subcycles of ZnO and 1 subcycle of SnO_2. To study how the film composition influences transistor properties, the following zinc-rich films were prepared: 3Z1T, 2.5Z1T, 2Z1T, 1Z1T, and 1Z2T. Here, 2.5Z1T is a modified recipe (3ZnO/1SnO_2/2ZnO/1SnO_2), which performed the best as a channel for transistors.

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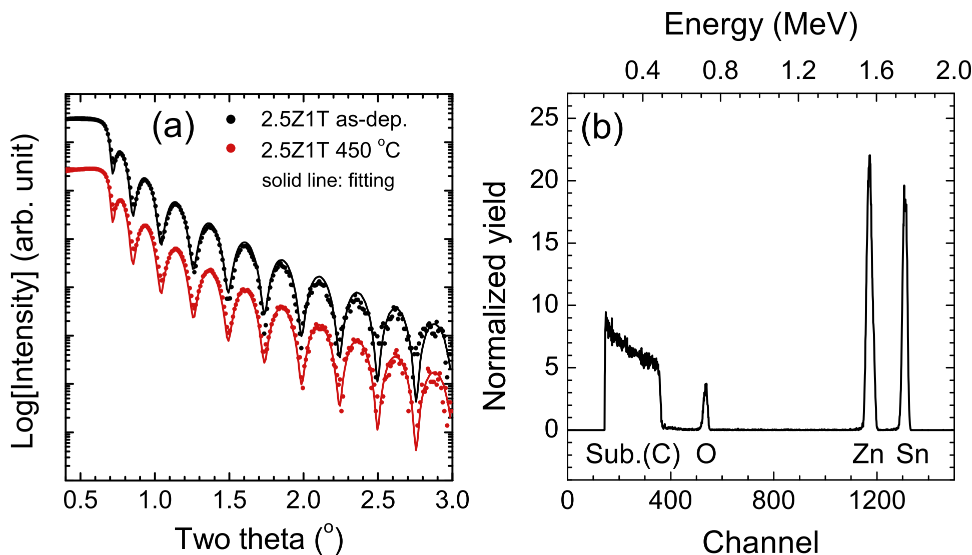

FIG. 1. (a) Representative x-ray reflectivity spectra for as-deposited and 450 °C-annealed 2.5Z1T ZTO on thermal oxide/Si substrate. Here, film thickness is ∼30 nm and the growth temperature is 170 °C. No significant change was observed after the annealing. The density was ∼5.3 g/cm^3 and RMS roughness was ∼0.8 nm. (b) RBS spectrum for as-deposited 2.5Z1T on a carbon substrate. The Zn/Sn ratio was estimated at 3.9.

Bottom-gate transistors were fabricated for the evaluation of ZTO channel layers grown on thermal oxide (∼120 nm)/highly doped *p*-Si (0.001 Ωcm) substrates. Channel thickness was ∼10 nm by varying the total number of supercycles based on the observed growth rate. Channel patterning was done by conventional photolithography and reactive ion etching with Ar/CH_4 mixed gas. Annealing in air followed for one hour at 450 °C. A transistor without high-temperature annealing was not turned off at zero bias of V_{GS} and exhibited a worse I_{ON}/I_{OFF} ratio of ∼10^2. E-beam evaporation was used for aluminum deposition on pre-defined source and drain areas, followed by liftoff. Twenty devices with various channel widths (W, 250–1000 μm) and lengths (L, 50–600 μm) were made on one substrate to investigate fringing electric field/sidewall effects.[21] Transmission line model (TLM) patterns were also included for contract resistance measurements.[22] The channel overlap with the source and drain was 150 μm. After annealing at 100 °C for 20 min in a hot oven to remove residual hydrocarbon and moisture, indium back contacts were made. Agilent 4156 C and 41501B were used for electrical analysis of the transistors. The measurements were done at room temperature in air under dark conditions. Field effect mobility was derived with V_G at 20 V and V_{DS} at 100 mV.[1]

Basic film properties were studied first. Film densities and compositions of ZTOs were measured by using x-ray reflectivity (PANalytical, X'Pert Pro) and Rutherford backscattering spectroscopy (RBS). Figure 1(a) shows representative reflectivity spectra of ∼30 nm-thick 2.5Z1T grown on thermal oxide. Film densities of ZTO layers grown at 170 °C were in the rage of 5.0–5.3 g/cm^3. No obvious change in film density, thickness and roughness was observed after the 450 °C-annealing, which indicates dense and stable films were grown. Figure 1(b) shows a representative RBS spectrum of a 2.5Z1T layer grown on a glassy carbon substrate (Ted Pella). Zinc to tin ratios (Zn/Sn) were measured to be 4.7, 3.9, 3.3, 2.2, and 0.9 for 3Z1T, 2.5Z1T, 2Z1T, 1Z1T, and 1Z2T, respectively. No other elements except Zn, Sn and O were detected. Optical transmission was measured by a spectrophotometer (Hitachi, U-4100). The average transmittance for wavelengths from 400 to 700 nm was measured for 2.5Z1T films with thicknesses of 10, 30 and 50 nm to be about 98, 90 and 82%, respectively, compared to an uncoated quartz reference.

The change in microstructure of ∼30 nm-thick ZTOs grown on thermal oxide as a function of annealing temperature in air was studied by using glancing-angle x-ray diffraction (incidence angle: 0.4°). Figure 2(a) shows representative spectra of 2.5Z1T. Broad peaks at around 34° are observed for as-deposited and annealed films up to 650 °C, which is characteristic of amorphous ZTO.[5,23] Crystallization occurred at 750 °C and the observed spectrum matched with cubic spinel Zn_2SnO_4.[23] When the surface morphology of ZTO films was examined by atomic force microscopy (AFM, Asylum, MFP-3D), phase separation was observed at an annealing temperature lower than the crystallization temperature. As shown in the inset of Fig. 2(b), particles (size: 200–500 nm, height: 60–80 nm, distance: 1–4 μm) were detected on the film surface. The phase separation temperature was dependent on the Zn/Sn ratio as summarized in Fig. 2(b). The temperature for phase separation increased with tin content. The sample with highest tin content, 1Z1T, did not show any sign of phase separation up to its crystallization temperature of 650 °C, which may be due to its having stoichiometry (Zn/Sn: 2.2) close to that of the Zn_2SnO_4 phase. Higher Zn concentration of this particle was revealed by energy dispersive x-ray spectroscopy (EDX), as shown in the elemental line profile of Fig. 2(c). Raman analysis confirmed that Zn-O bonding is the dominant chemical nature of the particle (data not shown). Annealing for transistor fabrication was limited to 450 °C based on these analyses.

Figure 3 shows the representative output (I_{DS}-V_{DS}) and transfer (log(I_{DS})-V_{GS}) curves for a 10 nm-thick 2.5Z1T channel (L: 70 μm, W: 1000 μm). The inset in Fig. 3(a) is an optical microscope image of the fabricated device. Hard saturation is clearly seen from the output curve, which suggests that the device behaves similarly to the conventional metal-oxide-semiconductor field effect transistor.[5,24] The shape of the curve near V_{GS} at 0 V is also convex, which indicates minimal current crowding at the source and drain contacts.[1,6,12] The measured specific contact resistance from the TLM pattern on this device was ∼0.6 Ωcm^2. Considering its

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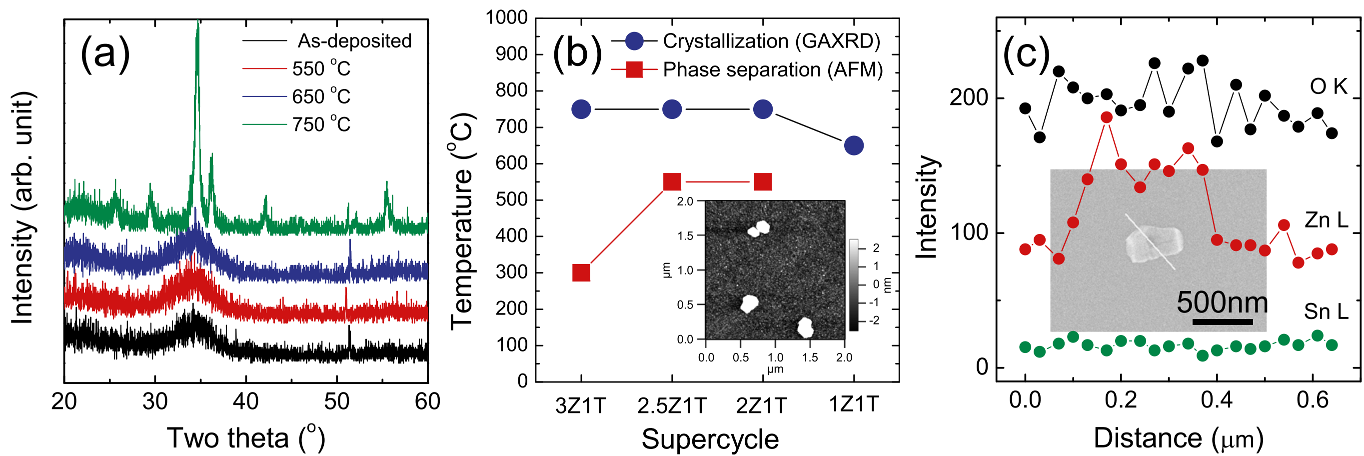

FIG. 2. (a) Glancing-angle x-ray diffraction of as-deposited and annealed 2.5Z1T ZTO films grown on thermal oxide/Si substrates (incidence angle: 0.4°). Crystallization occurred at 750 °C. (b) The crystallization (circles) and phase separation (squares) temperatures for ZTO layers with different compositions. Inset: An AFM image of a 550 °C-annealed 2.5Z1T ZTO film. No phase separation was observed for 1Z1T up to 650 °C. (c) EDX O, Zn, and Sn line profiles of the phase separated particle (inset image), which was analyzed as Zn-rich phase.

low carrier concentration of $\sim10^{15}/\mathrm{cm}^3$ after annealing at 450 °C (based on Hall measurements and sheet resistance from TLM), this value is in line with other ZnO-based oxides with similar carrier concentrations.[25,26] The transfer length was calculated to be ∼24–27 μm for the 2.5Z1T transistor.

It is noted from the transfer curve of Fig. 3(b) that the ZTO transistor operates in enhancement mode. The I_{ON}/I_{OFF} ratio was as high as $\sim10^9$–10^{10}, which is comparable to or better than other reports for well-behaved transistors.[9,11] The I_{ON}/I_{OFF} ratio derived from the transfer curve for V_{DS} of 20 V showed a clearly decreasing trend with a decreasing Zn/Sn ratio; it was $\sim10^9$–10^{10} for 3Z1T, 2.5Z1T, and 2Z1T, and it decreased to $\sim10^7$–10^8 and further to $\sim10^6$ for 1Z1T and 1Z2T, respectively. Turn-on voltage,[5] the gate voltage at the onset of the initial sharp increase in a transfer curve, was mainly at 0–3 V except for the 1Z2T transistor, which was largely negative-shifted (−9 V). The SS value was as low as 0.27 V/decade for the 2.5Z1T channel as shown in the inset of Fig. 3(b), and this value is comparable or better than other reports for ZTO transistors.[8,9,11] The minimum off-current was generally in the range of 10^{-13}–10^{-14} A, which is below the maximum level of 10^{-12} A for flat-panel displays.[1]

The Zn/Sn ratio clearly influenced the mobility of the transistors. The highest field effect mobility of ∼12–13 cm²/V·s was obtained for 3Z1T, 2.5Z1T, and 2Z1T channels as plotted in Fig. 4(a). Here, the mobility was derived from the transfer curve for V_{DS} of 0.1 V. As the Zn/Sn ratio decreases, mobility drops to ∼10 and ∼5 cm²/V·s for 1Z1T and 1Z2T transistors, respectively. McDowell *et al.* reported a similar decreasing trend of mobility with decreasing Zn/Sn ratio from ∼4 to 1 by the sputtering method.[8]

When ZTO layers were grown at 120 °C, which is near the lower end of the ALD window, lower mobilities of at most ∼3.4 cm²/V·s were obtained. Still, a similar trend of decrease with decreasing Zn/Sn ratio was observed. The I_{ON}/I_{OFF} ratio decreased to $\sim10^7$ in addition to the increased SS for Zn/Sn ratio of ∼3. Overall drastic worsening of transistor parameters was observed for 120 °C-grown 1Z2T as well. Based on these observations, it is concluded that higher Zn content leads to higher mobility when the Zn/Sn ratio is

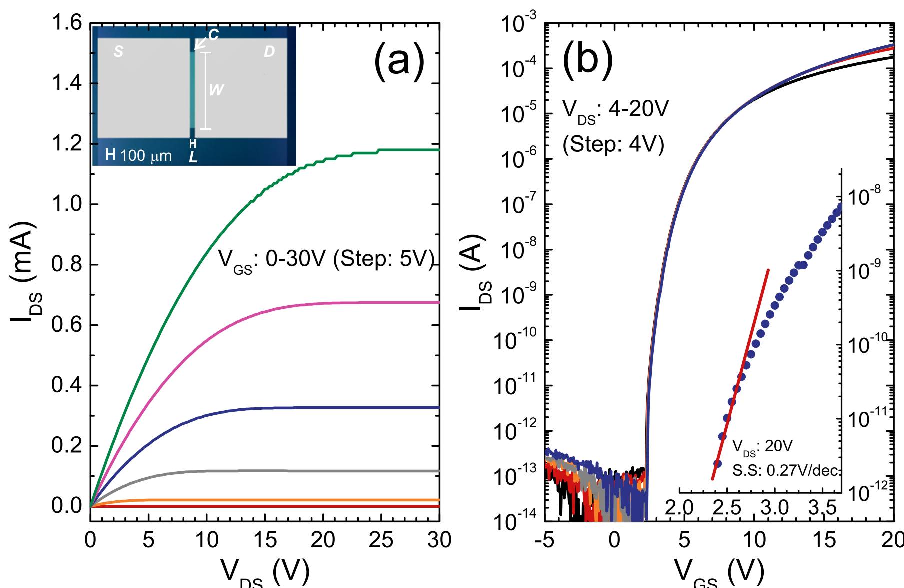

FIG. 3. (a) Representative I_{DS}-V_{DS} output characteristics of a transistor with 450 °C-annealed 2.5Z1T ZTO channel (L: 70 μm, W: 1000 μm). An optical microscope image of the fabricated transistor is shown as an inset. (b) Log(I_{DS})-V_{GS} transfer curve for the transistor. Inset is the enlargement for subthreshold swing determination at V_{DS} of 20 V. Here, sweep is 50 mV step. Subthreshold swing was 0.27 V/decade.

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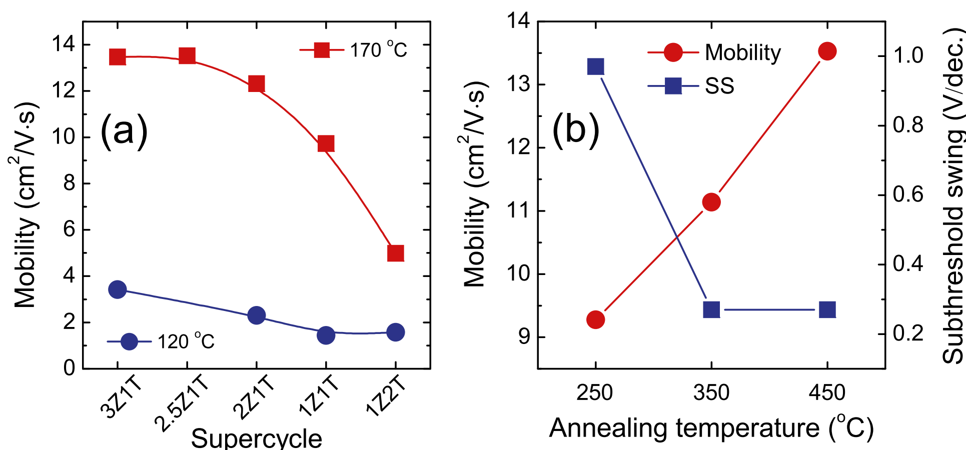

FIG. 4. (a) Field effect mobility for ZTO channels with various Zn/Sn ratios. Here, two different growth temperatures of 120 and 170 °C were compared. (b) Field effect mobility and subthreshold swing of transistors with 2.5Z1T channel as a function of annealing temperature.

larger than 1. It should be mentioned that although phase separation occurred for 3Z1T after annealing at 450 °C, comparable transistor properties to 2.5Z1T and 2Z1T channels were obtained. It appears that the influence of phase-separated ZnO particles on transistor operation is minimal as the current flow is close to semiconductor/insulator interface. No increase of field effect mobility with decreasing W/L from 20 to 1.67 was observed, which also indicates that the effect of fringing electric fields is negligible in our ZTO transistors.[21]

The channel mobility was influenced by annealing temperature. The change in mobility of 2.5Z1T channel for different annealing temperatures from 250 to 450 °C is plotted in Fig. 4(b). As the annealing temperature increases, higher mobility was obtained. This effect could be due to favorable rearrangement of channel materials. All three transistors exhibited similar I_{ON}/I_{OFF} parameters of $\sim10^9$–10^{10}; however, the SS of the 250 °C-annealed transistor was higher (0.97 V/decade) than that of the other two transistors (0.27 V/decade). This result suggests that fabrication of ALD-based ZTO transistors is compatible with most electronic device applications including some polymer substrates. Further improvement in the mobility of the transistors may be achieved by using a zinc precursor, such as zinc acetate ($Zn(CH_3COO)_2$), that is thermally stable at higher growth temperatures above 170 °C.[27]

The drive current density per unit width could be increased by depositing the transistors conformally over highly patterned substrates, such as arrays of parallel narrow trenches. Conformal ALD and CVD techniques are available to make the required insulator films, as well as conformal metal gates and contacts. This approach could boost the effective drive current by a large factor equal to the trench depth divided by the trench width.

In summary, transistors were demonstrated with amorphous zinc tin oxide as a channel layer grown by atomic layer deposition. The optimized composition was stable against phase separation and crystallization up to temperatures over 500 °C. Transistor parameters were highly dependent on film composition, and both growth and annealing temperatures. The highest electron mobility and drain current on-to-off ratio of $\sim$13 cm^2/V·s and $\sim10^9$–10^{10}, respectively, were obtained for 450 °C-annealed zinc-rich zinc tin oxides. The lowest subthreshold swing was 0.27 V/decade. Even for channels with a lower annealing temperature of 350 °C, mobility as high as $\sim$11 cm^2/V·s with a good subthreshold swing of 0.27 V/decade was obtained. The ALD method can provide highly uniform thickness and composition scalable over large areas, even on rough or structured substrates. Patterned films can potentially be grown using simple printing of inhibitors that prevent growth on undesired areas, without the need for any etching process.

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