Impact of ultrathin Al_2O_3 barrier layer on electrical properties of $LaLuO_3$ metal-oxide-semiconductor devices

Yiqun Liu,[1] Shaoping Shen,[2] Leonard J. Brillson,[2] and Roy G. Gordon[1,a)]
[1]*Department of Chemistry and Chemical Biology, Harvard University, Cambridge, Massachusetts 02138, USA*
[2]*Department of Electrical and Computer Engineering, Ohio State University, Columbus, Ohio 43210, USA*

(Received 6 January 2011; accepted 17 February 2011; published online 24 March 2011)

Temperature-dependent current-voltage measurements showed Poole–Frenkel conduction behavior through high-κ $LaLuO_3$ films made by atomic layer deposition on Si. The energy levels that trap electrons were around 0.66 eV below the conduction band and were identified as oxygen vacancy levels. Oxygen treatments were done to decrease oxygen vacancies but an interfacial layer formed and the interface state density (D_{it}) increased. Therefore, ultrathin Al_2O_3 was used to protect the interface during oxygen treatments. Electrical properties were improved and no interfacial layer developed. D_{it} was below 9×10^{11} eV^{-1} cm^{-2} and leakage was 5×10^{-4} A/cm^2 at 1 V for 1 nm equivalent oxide thickness. © *2011 American Institute of Physics*. [doi:10.1063/1.3563713]

High-κ dielectrics have been widely studied as alternative gate dielectrics to replace silicon dioxide for metal-oxide-semiconductor field-effect transistors (MOSFETs) and dynamic random access memories. Intel has employed hafnium-based dielectrics in high volume production at the 32 nm node.[1] However, the formation of a lower-κ interfacial layer (IL) during the hafnium-based dielectrics integration limits future scalability of Hf-based dielectrics.[2] Solutions should be found for future generations of devices to obtain equivalent oxide thickness (EOT) as low as 0.5 nm with an abrupt high-κ oxide/silicon interface while keeping a tolerable gate leakage current.

Lanthanum lutetium oxide ($LaLuO_3$) is identified as one of the most promising high-κ candidates. It fulfills the requirements of high dielectric constant ($\kappa\sim30$), large band gap (5.6 eV), and band offsets (2–2.5 eV),[3,4] and its amorphous phase is stable up to 1000 °C.[5] We have reported the potential of $LaLuO_3$ by atomic layer deposition (ALD) to reach small EOTs close to the International Technology Roadmap for Semiconductors requirements.[6] Nevertheless, the process still needs optimization since a high density of states form at the $LaLuO_3/Si$ interface, and the leakage needs to be reduced.

In this letter, the leakage conduction mechanism was studied by temperature-dependent current-voltage (J-E) measurements. A trap energy level was found based on the Poole–Frenkel (PF) conduction model and was identified as an oxygen vacancy level. Postdeposition anneal (PDA) in oxygen was applied to lower the concentration of oxygen vacancies. However, an IL formed between $LaLuO_3$ and the Si substrate, leading to an increase in EOT and deformed C-V curves. To prevent IL formation, an ultrathin Al_2O_3 barrier layer (0.4 nm) was added before $LaLuO_3$ deposition. Applying PDA in oxygen to the $LaLuO_3/Al_2O_3/Si$ stack improved the electrical properties of capacitors without causing any significant increase in EOT. Changes in defect densities were monitored by cathodoluminescence measurements, which showed that PDA reduced the number of oxygen vacancies and that Al_2O_3 decreased the defects derived from the IL.

Amorphous $LaLuO_3$ thin films were deposited from the precursors lanthanum tris(N,N'-diisopropylformamidinate), lutetium tris(N,N'-diethylformamidinate), and H_2O in a horizontal gas flow reactor. The lanthanum precursor was vaporized at 120 °C while the slightly more volatile lutetium precursor was kept at 115 °C. The temperature window for ALD growth was between 250 and 350 °C. The highest temperature, 350 °C, was chosen so that fewer hydroxyl groups should remain in the film. The deposition process was described elsewhere in detail.[7] Two kinds of substrates were used. One was hydrofluoric acid (HF)-last Si(100) with n-type resistivity 0.5–1 Ω cm, and the other was the same Si substrate with six ALD cycles of Al_2O_3 ($\sim$0.4 nm) deposited from trimethylaluminum and water at 300 °C in the same reactor chamber. After the deposition of $LaLuO_3$, some of the samples were subjected to PDA in oxygen by trapping 1 torr of oxygen gas in the reactor chamber for 10 min (exposure 6×10^8 L) at 300 °C. For electrical measurements, 15 nm ALD MoN was deposited in the same reactor at 300 °C as a protective layer and top metal electrode. Four types of dielectric stacks were studied. Samples A and B are as-deposited and oxygen-treated $LaLuO_3/Si$ stacks, respectively. Samples C and D are as-deposited and oxygen-treated $LaLuO_3/Al_2O_3/Si$ stacks, respectively. Au/Cr was then patterned into squares 100 μm$\times$100 μm in size by a lift-off process to serve as an etch mask and to enhance the conductivity of the top contact. Exposed MoN was then removed by CF_4/Ar reactive ion etching through the Au/Cr etch mask to form MOS capacitors. Pt/Pd alloy was sputtered on the backside for back contact.

Figure 1(a) shows temperature-dependent J-E characteristics for MOS capacitors of sample A with 6 nm $LaLuO_3$. The leakage current density (J) grew quickly with applied voltage (E) in the midfield region and increased strongly with temperature. The PF model was found to fit these data. PF conduction is due to field-enhanced thermal excitation of trapped electrons into the conduction band, and J-E data should follow the relationship[8–10]

a)Electronic mail: gordon@chemsitry.harvard.edu.

© 2011 American Institute of Physics

Downloaded 25 May 2011 to 128.103.149.52. Redistribution subject to AIP license or copyright; see http://apl.aip.org/about/rights_and_permissions

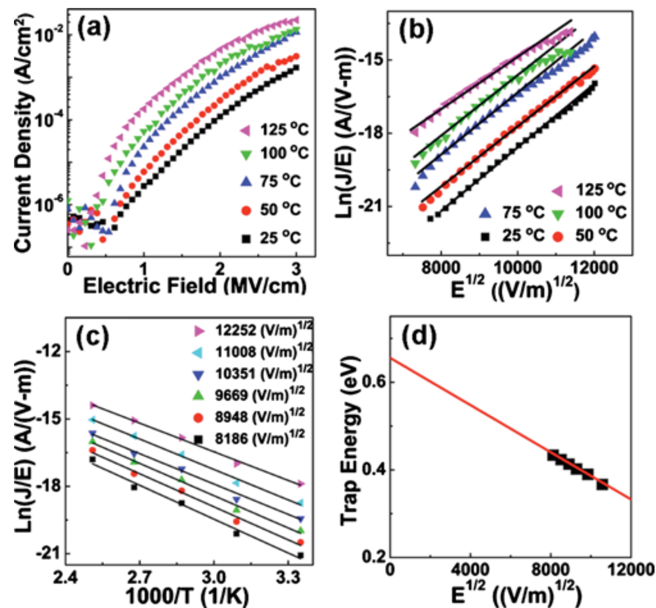

FIG. 1. (Color online) (a) Temperature-dependent J-E characteristics from MOS capacitors with 6 nm $LaLuO_3$. (b) Plots of ln(J/E) vs $E^{1/2}$ at various temperatures. (c) Plots of ln(J/E) vs 1/T at various electric fields. (d) A linear fit of trap energy levels as a function of electric field.

$$J \sim E \exp\left[\frac{-q(\Phi_B - \sqrt{qE/\varepsilon_0\varepsilon_r\pi}}{kT}\right], \quad (1)$$

where Φ_B is the trap energy level below the conduction band of the insulator and ε_r is the high-frequency dielectric constant (the square of the refractive index). The plots of ln(J/E) versus $E^{1/2}$ at various temperatures, as shown in Fig. 1(b), show linear behavior in the mid-field region, which agrees with the PF emission model. The refractive index is ~2.1, extracted from the slope of the curve measured at 25 °C, which is comparable to the optical refractive index measured at wavelength of 630 nm (1.9–2.0). ln(J/E) was plotted against 1/T and fitted to linear equations at various electric fields in order to extract the trap energy level [Fig. 1(c)]. The values of the slopes from the linear fits were then plotted against the corresponding electric fields, as shown in Fig. 1(d). The trap energy level of the dielectric at zero electric field was extrapolated from the y-intercept of the linear fit and was estimated to be 0.66 eV below the conduction band. This value matches well with one of the oxygen vacancy levels in $LaLuO_3$ calculated by Xiong and Robertson.[11] Oxygen vacancies have been identified as main sources of charge trapping and other problems for high-κ oxides. Our result provides evidence for oxygen vacancies as the origin of those trap levels, which can be one of the mechanisms for leakage.[10,12] Therefore, attempts were made to lower the oxygen vacancy concentration by oxygen treatments.

Figures 2(a) and 2(b) show C-V measurements of MOS capacitors of samples A and B at different frequencies (10 kHz, 100 kHz, and 1 MHz). Both capacitors have 6 nm $LaLuO_3$. An EOT of 1.24 nm and flatband voltage of 0.28 V were determined by fitting the measured data in Fig. 2(a) by the MISFIT simulation program (including quantum mechanical effects).[13] The estimated D_{it} is 2.5×10^{12} eV^{-1} cm^{-2} by fitting the curve including the small shoulder at 10 kHz. However, the electrical properties of $LaLuO_3$ MOS capacitors were degraded after O_2 treatment [Fig. 2(b)]. EOT was

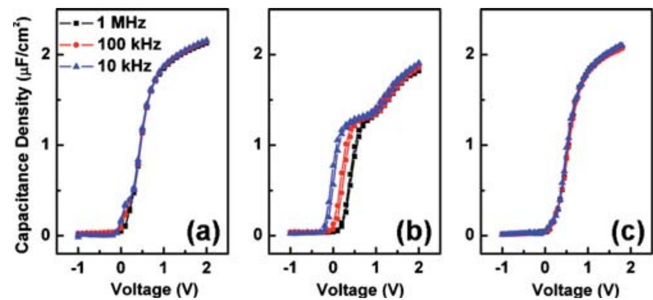

FIG. 2. (Color online) Capacitance-voltage characteristics of MOS capacitors of three types of samples (a) as-deposited $LaLuO_3$/Si, (b) oxygen-treated $LaLuO_3$/Si, and (c) as-deposited $LaLuO_3/Al_2O_3$/Si. All capacitors have 6 nm $LaLuO_3$.

increased to 1.5 nm, indicating that a thicker IL developed. The shoulder became higher and the simulation estimated an increased D_{it} of 1.5×10^{13} eV^{-1} cm^{-2}. Figures 3(a) and 3(b) show cross-sectional transmission electron micrographs (XTEMs) of samples A and B. The interface appears sharp for the as-deposited sample A while the oxygen treatment developed an IL around 0.8 nm thick in B. These results are consistent with the electrical analysis and the increased D_{it} is likely due to the IL. Therefore, an efficient O_2 diffusion barrier is necessary to protect the interface during oxygen treatments.

ALD Al_2O_3 ($\kappa\sim8$) was selected as the barrier between $LaLuO_3$ and Si and a 0.4 nm ultrathin layer (around two monolayers) was used in order not to increase the EOT of the whole stack by more than about 0.2 nm.[14,15] Figure 2(c) shows C-V measurements of sample C with 6 nm $LaLuO_3$. EOT is 1.25 nm and increased by only 0.8%, compared with sample A. The flatband voltage is shifted to 0.35 V due to negative fixed charges in Al_2O_3.[16] There is no shoulder in the low-frequency C-V curves and D_{it} is improved to below 9×10^{11} eV^{-1} cm^{-2}. This result suggests that the high density of interface traps in sample A resulted from the reaction of $LaLuO_3$ with Si. Our previous studies have shown that silicate was formed (~a monolayer) during the initial growth of ALD La_2O_3 on HF-last Si substrates by using *in situ* Fourier transform infrared spectroscopy,[17] although it cannot be clearly seen from the XTEM image in Fig. 3(a). We suspect that the interface states originate from the silicate IL and the Al_2O_3 barrier layer can remove those interface states by preventing silicate formation. The C-V characteristics of oxygen-treated sample D are similar to the results shown in Fig. 2(c), which suggests that Al_2O_3 can preserve a good interface during oxygen treatments. The XTEM image of sample D reveals the presence of an amorphous $LaLuO_3$ layer on an amorphous Al_2O_3 layer with a uniform thickness of ~0.4 nm in Fig. 3(c). The Al_2O_3/Si interface is sharp at

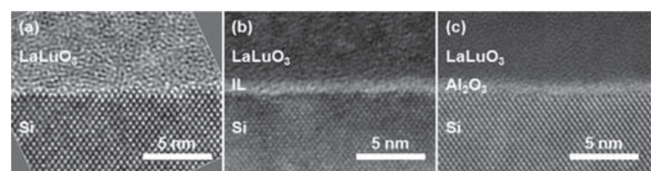

FIG. 3. XTEM images of (a) the as-deposited $LaLuO_3$/Si stack showing a sharp interface between oxide and Si, (b) the oxygen-treated $LaLuO_3$/Si stack showing an IL of ~0.8 nm between $LaLuO_3$ and Si, and (c) the oxygen-treated $LaLuO_3/Al_2O_3$/Si stack.

Downloaded 25 May 2011 to 128.103.149.52. Redistribution subject to AIP license or copyright; see http://apl.aip.org/about/rights_and_permissions

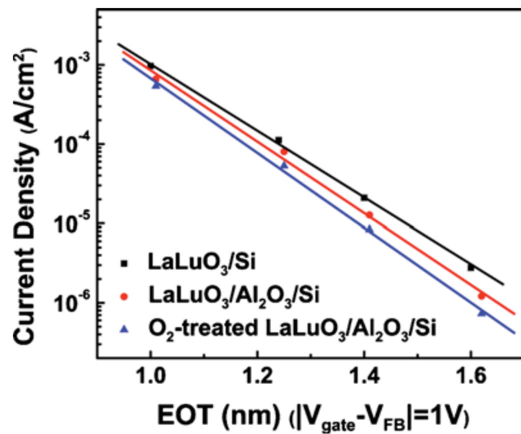

FIG. 4. (Color online) Comparison of gate leakage current density as a function of EOT between MOS capacitors of as-deposited $LaLuO_3/Si$, as-deposited, and O_2-treated $LaLuO_3/Al_2O_3/Si$ at 1 V gate bias.

the atomic scale and does not show any change compared with the interface without oxygen treatments (XTEM image of sample C not shown). These results confirm the protective role of the ultrathin Al_2O_3 layer.

Depth-resolved cathodoluminescence spectroscopy (DRCLS) was used to detect the defect energies and densities in these dielectric stacks.[18,19] The experiments and results were described in detail elsewhere.[20] The band gap of $LaLuO_3$ was determined to be ~5.5 eV. Defect peaks at 4.2 and 4.7 eV above the valence band were identified as oxygen vacancy levels, where 4.7 eV is close to the trap energy level estimated from the electrical measurements. There was also a peak at 3.8 eV. Oxygen treatments reduced the peak intensities at 4.2 and 4.7 eV, presumably by filling the oxygen vacancies. But the peak intensity at 3.8 eV increased, which suggests that this defect level originated from the IL and the defect density becomes higher when a thicker IL is formed. The 3.8 eV peak was strongly reduced by adding the ultrathin Al_2O_3 barrier and it did not increase by oxygen treatments. These results confirm that the ultrathin Al_2O_3 layer protects the interface from silicate formation and that oxygen treatment can reduce the oxygen vacancies.

Figure 4 compares how the leakage current density increases with decreasing EOT for different structures. The logarithmic plot of the leakage current rises linearly with shrinking EOT. The Al_2O_3 barrier layer reduced the leakage current by a factor of 2 for the same EOT, and oxygen treatment further decreased the leakage by filling oxygen vacancies in $LaLuO_3$. The lowest leakage current density of 5×10^{-4} A/cm^2 was achieved at 1 V gate bias with EOT $=1$ nm for O_2-treated $LaLuO_3/Al_2O_3/Si$ stacks. The oxygen treatment is efficient in curing oxygen vacancies in $LaLuO_3$ without damaging the interface when it is protected by an Al_2O_3 barrier layer.

In summary, a trap energy level of $LaLuO_3$ was found 0.66 eV below the conduction band from the temperature-dependent leakage current, fit to the PF emission model. The trap was identified as one of the oxygen vacancy levels in $LaLuO_3$. However, PDA in oxygen alone deteriorated the device properties (increased D_{it}) because it formed a silicate IL. Therefore, an ultrathin Al_2O_3 barrier layer was added between $LaLuO_3$ and Si prior to O_2 treatment. IL-free dielectrics were achieved with well-behaved electrical characteristics at EOT=1 nm. The leakage current densities were in the range of 0.1–1 mA/cm^2 and D_{it} is below 9×10^{11} eV^{-1} cm^{-2}. DRCLS confirmed that oxygen treatment can reduce the oxygen vacancies and an ultrathin Al_2O_3 interlayer can prevent formation of a defective IL. These results suggest the usefulness of the O_2-treated $LaLuO_3/Al_2O_3/Si$ stack for future low-power MOSFETs.

Dow Electronic Materials supplied the precursors for lanthanum and lutetium. Part of this work was performed at the Center for Nanoscale Systems (CNS) at Harvard University. Harvard CNS is a member of the National Nanotechnology Infrastructure Network (NNIN). OSU authors gratefully acknowledge support from NSF MRSEC Grant No. DMR-0820414 and ONR Grant No. N00014-10-1-0896.

[1]P. Packan, S. Akbar, M. Armstrong, D. Bergstrom, M. Brazier, H. Deshpande, K. Dev, G. Ding, T. Ghani, O. Golonzka, W. Han, J. He, R. Heussner, R. James, J. Jopling, C. Kenyon, S. H. Lee, M. Liu, S. Lodha, B. Mattis, A. Murthy, L. Neiberg, J. Neirynck, S. Pae, C. Parker, L. Pipes, J. Sebastian, J. Seiple, B. Sell, A. Sharma, S. Sivakumar, B. Song, A. St. Amour, K. Tone, T. Troeger, C. Weber, K. Zhang, Y. Luo, and S. Natarajan, presented at the 2009 IEEE International Electron Devices Meeting (IEDM, 2009) (unpublished).
[2]J. Robertson, Rep. Prog. Phys. **69**, 327 (2006).
[3]J. M. J. Lopes, M. Roeckerath, T. Heeg, E. Rije, J. Schubert, S. Mantl, V. V. Afanas'ev, S. Shamuilia, A. Stesmans, Y. Jia, and D. G. Schlom, Appl. Phys. Lett. **89**, 222902 (2006).
[4]D. G. Schlom and J. H. Haeni, MRS Bull. **27**, 198 (2002).
[5]M. Roeckerath, T. Heeg, J. M. J. Lopes, J. Schubert, S. Mantl, A. Besmehn, P. Myllymäki, and L. Niinistö, Thin Solid Films **517**, 201 (2008).
[6]H. T. Wang, J. J. Wang, R. Gordon, J. S. M. Lehn, H. Z. Li, D. Hong, and D. V. Shenai, Electrochem. Solid-State Lett. **12**, G13 (2009).
[7]Y. Liu, M. Xu, J. Heo, P. D. Ye, and R. G. Gordon, Appl. Phys. Lett. **97**, 162910 (2010).
[8]S. M. Sze, *Physics of Semiconductor Devices*, 2nd ed. (Wiley, New York, 1981).
[9]S.-J. Ding, J. Xu, Y. Huang, Q.-Q. Sun, D. W. Zhang, and M.-F. Li, Appl. Phys. Lett. **93**, 092909 (2008).
[10]C.-H. An, M. S. Lee, J.-Y. Choi, and H. Kim, Appl. Phys. Lett. **94**, 262901 (2009).
[11]K. Xiong and J. Robertson, Microelectron. Eng. **86**, 1672 (2009).
[12]K. B. Jinesh, Y. Lamy, E. Tois, and W. F. A. Besling, Appl. Phys. Lett. **94**, 252906 (2009).
[13]G. Apostolopoulos, G. Vellianitis, A. Dimoulas, J. C. Hooker, and T. Conard, Appl. Phys. Lett. **84**, 260 (2004).
[14]R. M. C. de Almeida and I. J. R. Baumvol, Surf. Sci. Rep. **49**, 1 (2003).
[15]L. Becerra, C. Merckling, M. El-Kazzi, N. Baboux, B. Vilquin, G. Saint-Girons, C. Plossu, and G. Hollinger, J. Vac. Sci. Technol. B **27**, 384 (2009).
[16]M. Cho, H. B. Park, J. Park, S. W. Lee, C. S. Hwang, J. Jeong, H. S. Kang, and Y. W. Kim, J. Electrochem. Soc. **152**, F49 (2005).
[17]J. Kwon, M. Dai, M. D. Halls, E. Langereis, Y. J. Chabal, and R. G. Gordon, J. Phys. Chem. C **113**, 654 (2009).
[18]J. Zhang, S. Walsh, C. Brooks, D. G. Schlom, and L. J. Brillson, J. Vac. Sci. Technol. B **26**, 1466 (2008).
[19]S. Walsh, L. Fang, J. K. Schaeffer, E. Weisbrod, and L. J. Brillson, Appl. Phys. Lett. **90**, 052901 (2007).
[20]S. Shen, Y Liu, R. G. Gordon, and L. J. Brillson, "Impact of Ultrathin Al_2O_3 Diffusion Barriers on Defects in High-*k* $LaLuO_3$ on Si," Appl. Phys. Lett. (submitted).

Downloaded 25 May 2011 to 128.103.149.52. Redistribution subject to AIP license or copyright; see http://apl.aip.org/about/rights_and_permissions