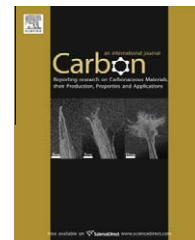


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Three dimensional solid-state supercapacitors from aligned single-walled carbon nanotube array templates

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ABSTRACT

We demonstrate the fabrication of solid-state dielectric energy storage materials from self-assembled, aligned single-walled carbon nanotube arrays (VA-SWNTs). The arrays are transferred as intact structures to a conductive substrate and the nanotubes are conformally coated with a thin metal-oxide dielectric and a conductive counter-electrode layer using atomic layer deposition. Experimental results yield values in agreement with those obtained through capacitive modeling using Al_2O_3 dielectric coatings ($C > 20 \text{ mF/cm}^2$), and the solid-state dielectric architecture enables the operation of these devices at substantially higher frequencies than conventional electrolyte-based capacitor designs. Furthermore, modeling of supercapacitor architectures utilizing other dielectric layers suggests the ability to achieve energy densities above 10 W h/kg while still exhibiting power densities comparable to conventional solid-state capacitor devices. This device design efficiently converts the high surface area available in the conductive VA-SWNT electrode to space for energy storage while boasting a robust solid-state material framework that is versatile for use in a range of conditions not practical with current energy storage technology.

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1. Introduction

The demand for energy storage and energy production is growing in parallel to a global population increase and successive rapid industrialization. The combination of a technologically advanced modern society and predictions of a future global energy crisis demands the implementation and design of new low-cost, highly efficient, and multifunctional frameworks for energy storage. As a result, energy storage systems: batteries, fuel cells, and supercapacitor technologies, are being adapted and optimized with nanostructured components [1–5]. The promise of nanomaterials for such energy

storage applications is to enhance the energy (or power) density, and the overall performance of the device relative to the cost. This results in cost-effective and smaller energy storage systems that appeal to both stationary and portable energy storage solutions.

Of all storage media, electrochemical energy storage systems have emerged as being the most promising for the future energy challenge [6–8]. In the particular case of supercapacitors, electric double-layer capacitors (EDLCs) have been studied now for over 60 years, with advanced designs including the use of high surface area electrodes such as single-walled carbon nanotubes and other high surface area carbons, with

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many such designs currently being developed on an industrial front [8]. The simple mechanism by which EDLC devices operate is by the generation of an electric double layer at the interface between the electrode material and the electrolyte when a voltage is applied. This means that energy storage in this device architecture is directly related to both the electrode surface area on which a double layer can form as well as the electrolyte mobility to that surface. Compared to batteries, EDLCs yield substantially greater power density, but with a markedly lower energy density. Until now, some of the most efficient EDLC designs have reported energy densities greater than 70 W h/kg [2], but most supercapacitors have been reported with energy densities between 1 W h/kg and 10 W h/kg [3,5,9–11]. Although these results are promising, EDLCs have numerous drawbacks for robust and integrated energy storage systems. Although significant progress has been made in determining electrolytes that are stable over a wide variety of conditions, the stability of the electrolyte in an EDLC under different operating conditions limits the versatility of such devices. For example, the use of these devices in a satellite in space, under the hood of an automobile, or connected to a solar panel in the desert would all require different electrolytes and safety considerations for use. In addition, current state-of-the-art energy storage systems for devices, such as MEMS or solid-state on-chip components, still integrate materials with classical dielectric capacitor architectures, since these material frameworks can be easily integrated into the device design despite their extremely low energy densities in comparison to EDLCs. Although capacitor designs, such as those integrated into DRAM, appeal toward such technology, such devices are typically embedded into heavy chips using top-down processes, limiting their use for devices requiring high specific energy density for stand-alone storage systems. Finally, due to the use of an electrolyte, EDLC device design is not load-bearing, which also limits its use in multifunctional energy storage applications, and the response rate of the EDLC device is typically slow (typically seconds) which limits the window for available energy storage systems that such materials can be utilized with. Although recent studies have demonstrated response times down to 20 ms [12], the use of a solid-state architecture is more tailored to such high frequency device performance.

Here, we demonstrate the experimental design of an energy storage material framework that combines the concept of the conventional solid-state capacitor architecture with the high surface area electrode that permits the comparably large energy density in an EDLC device. As a primary electrode in this device, we utilize vertically aligned single-walled carbon nanotube arrays (VA-SWNTs) that provide an excellent template to fabricate such an energy storage material. These ultra-high surface area self-assembled materials feature between ~5% and 7% carbon density [13] and conduction properties comparable to conventional metals along their length. To construct energy storage devices, we utilize atomic layer deposition (ALD) to build up thin nanoscale dielectric layers on the surface of the nanotube bundles in the arrays, and subsequently use ALD to coat a conformal counter-electrode on the dielectric material. In comparison to EDLC devices, this device architecture yields a robust load-bearing energy storage material framework that is versatile for many

different applications. The use of solid-state dielectrics enables potential operation at higher voltages (depending on the dielectric material), stability in a wide range of operating conditions, and the capability to store energy at a higher response rate (i.e. high frequencies). Additionally, comparing this architecture to other solid-state energy storage materials described thus far, this material architecture yields a substantially higher surface area that is well-suited for such a device template with the SWNT self-assembly during growth eliminating the need for any material processing prior to ALD coating.

Therefore, we discuss herein the first proof-of-principle results for this device architecture utilizing Al_2O_3 as the dielectric material in addition to supportive modeling to demonstrate the viability of this dielectric capacitor architecture. We demonstrate the correlation between experimentally measured capacitance and modeled capacitance for the SWNT- Al_2O_3 system, and further predict a material framework that can yield both high power and high energy densities utilizing better dielectric materials and optimized SWNT array geometries.

2. Experimental details

2.1. Vertically aligned SWNT growth and post-growth treatment

Vertically aligned SWNT growth was achieved using a water-assisted, low pressure (1.4 Torr) synthesis technique described in detail elsewhere [13,14]. Synthesis temperatures of 750 °C, catalyst layers composed of 0.5 nm Fe/10 nm $\text{Al}_2\text{O}_3/\text{SiO}_2/\text{Si}$, and rapid reduction with atomic hydrogen were all used as key ingredients to the effective growth of aligned SWNT arrays. Although multi-walled carbon nanotubes (MWNTs) would also be effective in this device framework, MWNT arrays typically have lower densities (<1% vs. >5% for SWNTs) and hence lower specific surface area, and often exhibit high levels of amorphous carbon and metal impurities that impact device performance.

Following growth, the aligned SWNT are transferred to flat Cu substrates by utilizing a thin Ti/Au layer deposited on both the Cu substrate and the SWNT array, and sintering these layers together under Ar at 700–750 °C [15]. This general process is illustrated in Fig. 1, where the Ti acts as an adhesion layer and the Au layer acts to form a robust mechanically stable electrical interface between the SWNT arrays and the Cu electrode. In this SWNT array material, the SWNTs arrange into bundles due to the strong van der Waals interaction energy between tubes in the array, and the close-packed spacing of catalyst particles on the growth substrates which causes tubes to bundle following nucleation. These bundles are found to be ~15–20 nm in diameter, on average, based on TEM characterization, but polydisperse in nature. Although an optimized supercapacitor material may involve control of bundle diameter in this material (Supplementary data), it is not clear how much control of bundle diameter can be achieved in the growth process. In order to facilitate the SWNT conduction properties, the transferred SWNT array is placed in a glass petri dish next to a watchglass filled with

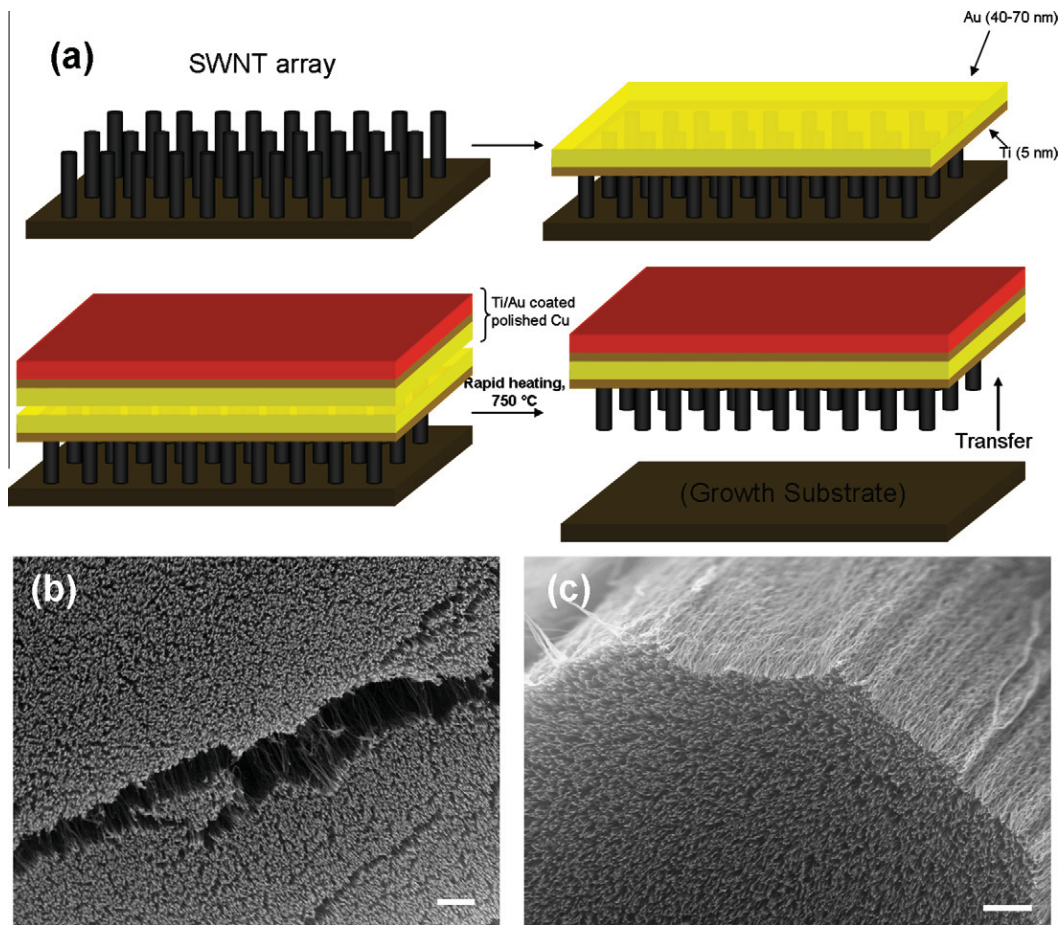


Fig. 1 – (a) Scheme depicting the process by which the VA-SWNT arrays are transferred from the growth substrate to a conductive substrate on which the supercapacitors are fabricated. (b,c) SEM images of VA-SWNTs directly following transfer to a conductive substrate. Scale bar = 1 μm .

fuming H_2SO_4 and covered overnight in a fume hood. In this way, H_2SO_4 vapors penetrate and p-dope the SWNT array [16] without resulting in capillary-induced rearrangement of the SWNT array commonly observed after liquid exposure. More information on this approach is available in the Supplementary data.

2.2. Supercapacitor fabrication from atomic layer deposition

In order to form the nanocapacitor arrays, metal-oxide atomic layer deposition (ALD) was utilized to coat a dielectric and conductive counter-electrode on the sidewalls of the SWNT in bundles to form a coaxial nanocapacitor having both a thin dielectric and conductive layer coating. Although numerous dielectric materials can be coated using ALD, Al_2O_3 coating using trimethylaluminum vapor (TMA) has been one of the premier chemistries for ALD and therefore our choice for this proof-of-concept device architecture. This was achieved by using alternating exposure to NO_2 gas with exposure to TMA to first functionalize SWNT bundles and then coat them [17,18]. A conformal coating of alumina, the dielectric layer for the nanocapacitor devices, is deposited on the outside of the SWNT bundles by ALD at 250°C . In order to make TMA and H_2O vapor effectively diffuse into the SWNT arrays, large

exposures of 20 Torr s for TMA and 39 Torr s for H_2O are used for each ALD cycle. Following this, the dielectric coated SWNT bundles are further conformally coated with 20 nm Al-doped ZnO using alternating layers of Al_2O_3 (1 cycle of TMA vapor and H_2O vapor) and ZnO (24 cycles of diethylzinc (DEZ) vapor and H_2O vapor). Large exposures of 38 Torr s for DEZ, 20 Torr s for TMA and 39 Torr s for H_2O are used for every ALD cycle. The Al-doped ZnO layer forms a conductive counter-electrode for the device, with a measured resistivity of $3.6 \times 10^{-3} \Omega \text{ cm}$ with the thicknesses and architectures deposited here that is sufficient to provide the function of a counter-electrode within the SWNT array to the top-contact metal. It should be noted that for successful device performance, a brief O-plasma treatment was applied between the dielectric and counter-electrode coating. The purpose of this is to selectively etch any SWNT bundle segments that exhibit coating defects (uncoated) that leave them exposed to the conductive Al-ZnO layer to short the device. This was found effective in most cases to transform the device response from that of a resistor to that of a filter.

2.3. Impedance analysis

Impedance analysis was carried out on a Quadtech 7000 series LCR meter capable of operation between 20 Hz and

1 MHz. For each point shown in Fig. 4, at least three points are recorded with the maximum possible averaging cycles allowed by the LCR meter, yielding standard deviations in measurements smaller than the size of the points in nearly all cases, and hence not included in Fig. 3. Detailed discussion of analysis of impedance data via equivalent circuit models is described at length in the supplementary information.

3. Results and discussion

As depicted in Fig. 2a, SWNT dielectric capacitors are fabricated from VA-SWNT arrays [13,14] having thicknesses of 20–50 μm , transferred to conductive surfaces [15,19], H_2SO_4 vapor-doped, and coated using ALD [17,18]. A thin conformal coating of Al_2O_3 (15–40 nm), and subsequent coating of Al-doped ZnO (20 nm) serve as the dielectric and counter-electrode material for these devices. This forms a metallic SWNT–insulator–metal nanocapacitor architecture producing a solid-state capacitor device. Following an initial ALD coating of Al_2O_3 (10 nm), the VA-SWNT were exposed to a 30 s oxygen plasma etch to mitigate any coating defects that could lead to device shorting. Following this, the devices were further coated with additional Al_2O_3 and Al-doped ZnO layers. Bright field transmission electron microscope images (Fig. 2b and c) depict this architecture for individual nanocapacitors, with evident differences in contrast between the SWNT, alumina, and conductive (darker) Al-doped ZnO conformal layer. In Fig. 2b, a typical SWNT bundle (diameter ~ 15 nm) is

conformally coated with a ~ 25 nm thick layer of alumina. In Fig. 2c and a ~ 20 nm bundle is coated with ~ 45 nm of alumina and ~ 20 nm of Al-doped ZnO. In the latter image, the SWNT bundle structure is difficult to resolve due to the greater nanocapacitor diameter, but still apparent upon close inspection. These images confirm the SWNT–insulator–metal concept of Fig. 2a and provide the basis for device characterization and calculations discussed herein.

Shown in Fig. 3 is a series of scanning electron microscope (SEM) images of SWNT nanocapacitor networks at different magnifications. Low magnification SEM (Fig. 3a and b) confirms the uniform penetration of the ALD coating into the bulk of the SWNT array, whereas higher magnification SEM (Fig. 3c) confirms the homogeneity in nanocapacitor diameter (~ 120 nm) agreeing well with expected ALD coating thickness. Extensive destructive and non-destructive imaging of the SWNT–dielectric interface material was carried out to ensure that the ALD coating process within the SWNT array was uniform and homogenous on the inner portions of the SWNT arrays. Due to the high precursor pressures utilized in this work, along with the self-limiting nature of the ALD process, we found this to be achieved utilizing the previously discussed conditions. It should be noted that ALD is a technique that is well-suited for this 3-D material architecture as it facilitates a layer-by-layer building of a material that only depends on the ability of the precursor to reach the reactive hydroxyl site. Metal-oxide coating through ALD on the inner portion of the VA-SWNT material is apparent in Fig. 3a and b by

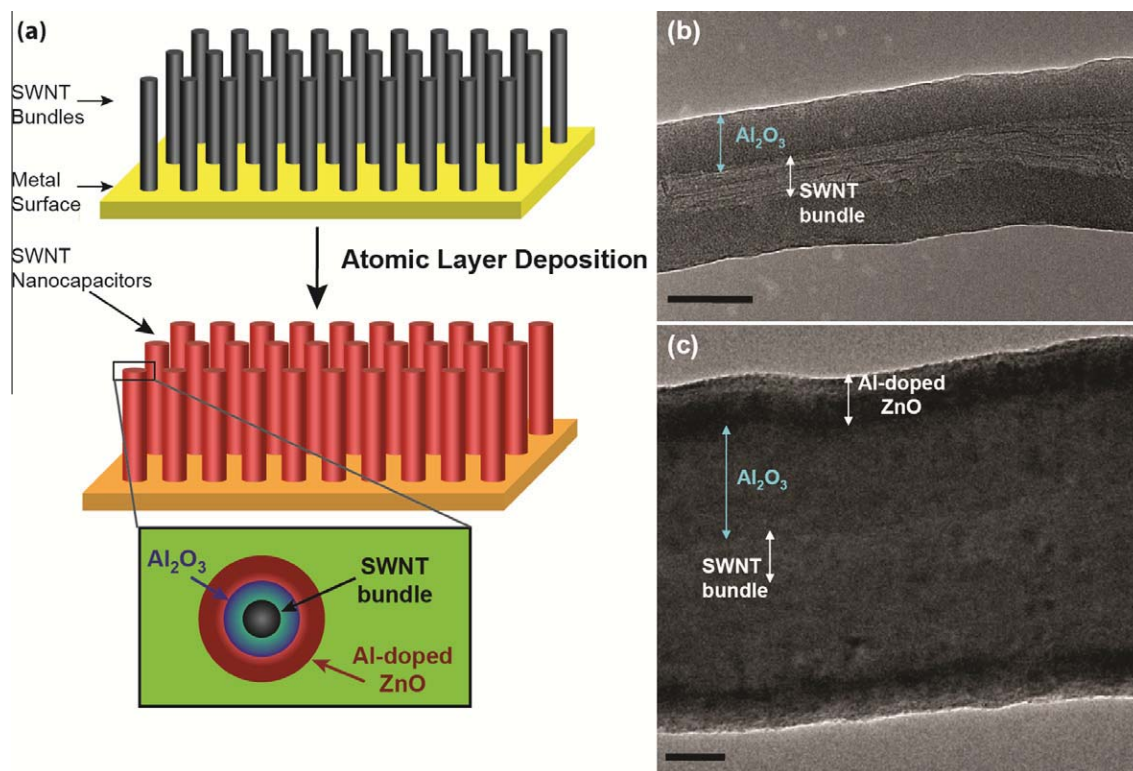


Fig. 2 – (a) Scheme of concept for SWNT supercapacitor devices. At the bottom of the scheme, a diagram of the coaxial nature of the nanocapacitors is depicted. (b,c) Bright field TEM images of bundles of SWNT coated with a conformal sheath of alumina, and a conformal sheath of alumina and an outer sheath of Al-doped zinc-oxide. Due to the conductive nature of the Al-doped ZnO, the coaxial structure can be identified and labeled based on the contrast of the layers in the TEM images. Note: scale bar = 30 nm.

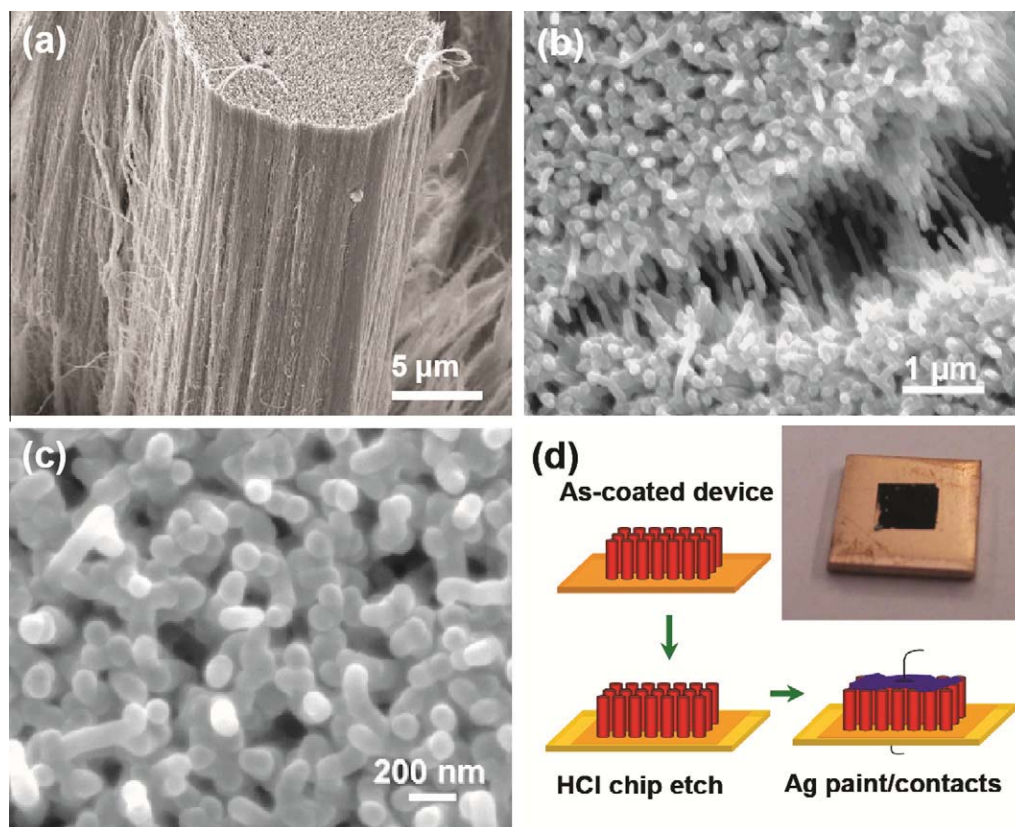


Fig. 3 – (a–c) SEM images of SWNT bundles coated with alumina and Al-doped zinc-oxide at three different (increasing) magnifications. (d) Picture of an as-coated device, and a scheme depicting the process by which devices are contacted with electrodes for electrical testing. Inset in (d) is a photograph of an as-prepared device.

comparing the morphology of the coated SWNTs to those shown elsewhere for the as-grown SWNT arrays. Furthermore, whereas bundles are evidently only ~ 20 nm in thickness in the uncoated SWNT arrays, the coated bundles uniformly have diameters often exceeding 100 nm, and with a thickness consistent with that expected from the respective oxide layer coating thicknesses in addition to the SWNT bundles. Following the ALD coating procedure, the devices are prepared for electrical characterization by applying a top electrical contact to the counter-electrode using Ag paint (Fig. 3d). The Al-ZnO layer on the edges of the Cu chip are dissolved by swabbing with 1 M HCl to isolate the conductive counter-electrode from the bottom electrical contact to prevent device shorting.

The capacitance of these devices is extracted from impedance analysis using a standard LCR meter (Fig. 4a and b). Two individual approaches were employed for measuring device capacitance: (i) measuring the full frequency dependent complex impedance and employing circuit theory to construct an equivalent circuit to extract capacitance, and (ii) assumption of a simple equivalent circuit and direct calculation of the frequency dependent capacitance via the LCR meter. As depicted in Fig. 4a, the device frequency response of the impedance, $|Z|$, is representative of a band-pass filter, and can be modeled with an equivalent RLC series circuit having a leakage resistance in parallel with the capacitor (solid line, Fig. 4a). While this provides a good fit to Z ($C = 13$ mF/cm³), no simple

lumped element circuit model is found to be capable of fitting the full complex valued impedance data (both Z and ϕ simultaneously). This is expected to be related to dispersion effects arising from device geometry and distributed capacitance, which has been proposed in other solid-state capacitor systems [20]. However, variations of acceptable equivalent circuit models is found to result in little difference of effective net capacitance, with all fit values between 6 mF/cm³ and 13 mF/cm³ for different analysis techniques (see supplementary information (SI)). Nonetheless, the best fitting simple circuit model for Z and ϕ simultaneously is a series RC circuit with a parallel leakage resistance component, where $R_{leakage} \gg R_{series}$. This yields $C = 6$ mF/cm³ for this device. With this circuit model, the frequency dependent device capacitance can be directly calculated from the LCR meter for this specific device, as shown in Fig. 4b (for both volumetric and planar capacitance). At 20 Hz, $C = 23$ mF/cm³ and rapidly falls to ~ 6 mF/cm³ above 100 Hz. As noted earlier, this behavior is believed to be a result of dispersion in the device. Assuming SWNT array density of 50 mg/cm³ [13,14], and maximum measured operating voltages between 1 V and 3 V (see supplementary information SI), this yields specific capacitance (C_{sp}) near 0.5 F/g (carbon), and energy density between 0.05 and 0.5 W h/kg – the latter being a moderate value that is comparable to a low-end CNT-based EDLC devices [3,9–11]. On the basis of total weight (Al₂O₃, Al-doped ZnO included), this yields C_{sp} near 0.1–0.13 F/g, with energy density between

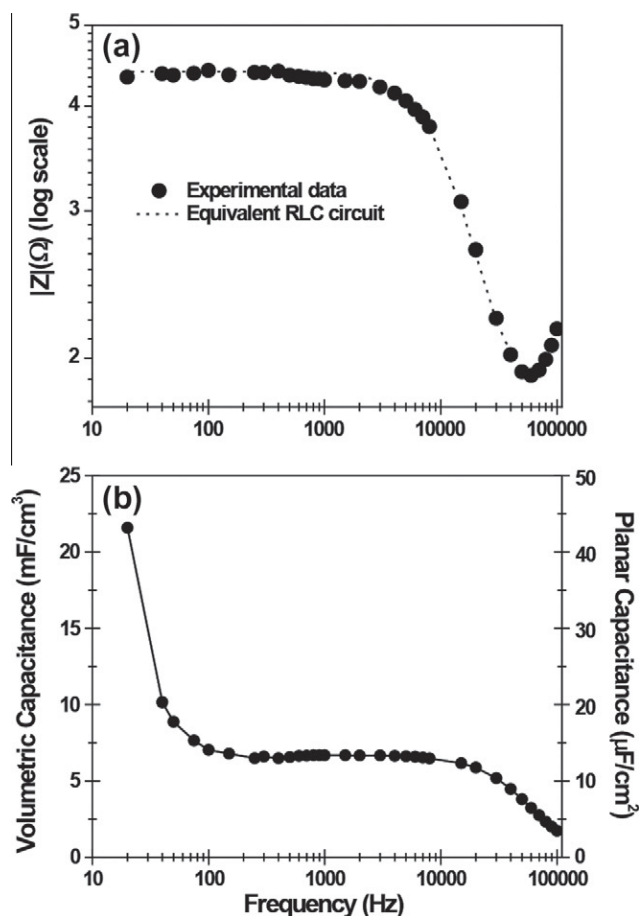


Fig. 4 – (a,b) Frequency response of the impedance, Z , and capacitance as measured directly from an LCR meter. Note the fit in a is an equivalent RLC circuit model (described in text and SI) that gives the best fit to the experimental data. The capacitance in b is shown in both volumetric capacitance (F/cm^3) and planar capacitance (F/cm^2).

0.01 and 0.13 Wh/kg. For lightweight energy storage and industrially packaged devices, this latter consideration is important. Although the mass density of the solid-state dielectric is typically larger than that of the electrolyte used in an EDLC device, the amount of electrolyte used in EDLC devices volumetrically inefficient and results in the addition of excessive electrolyte to ensure proper access of the electrolyte to the high surface area electrode. In this way, this solid-state dielectric approach is more controlled and could potentially be tuned to yield lightweight energy storage by tuning the performance as a function of the thickness of coated materials (see supplementary information SI).

Despite the greater versatility in use of this device architecture, an additional key feature to the solid-state device is the energy storage capability at higher response rates, or higher frequencies. As shown in Fig. 4, the volumetric capacitance retains $\sim 25\%$ of its low-frequency (i.e. DC) value at frequencies up to 20 kHz ($6 \text{ mF}/\text{cm}^3$). In comparison to a standard electrolyte-based energy storage device which are constrained to slow response times (typically 0.1–10 s), the solid-state energy storage architecture represents a key advantage since high frequency device performance can be

obtained. Although the long charging and discharging times of EDLCs are well-suited for many applications, the use of higher frequency energy storage materials is especially useful for on-chip or integrated device technology. In such device architectures, solid-state energy storage designs are also more easily integrated into the fabrication techniques implemented to generate other on-chip components and this route represents an exciting approach to efficient energy storage in such a situation.

It should be noted that several devices were measured to have low-frequency capacitances between $0.1 \text{ mF}/\text{cm}^3$ and $23 \text{ mF}/\text{cm}^3$, with frequency response similar to Fig. 4. H_2SO_4 doping before ALD coating appears a critical factor in achieving the maximum capacitance, which may result from doping induced carrier-density enhancement in the SWNT electrodes [21]. Order-of-magnitude device-to-device variation of capacitance measurements is a key indication that engineering approaches to improve device architecture and coating process can influence optimal device performance, and future work is planned to focus on optimizing this device architecture for energy storage applications. However, in order to better

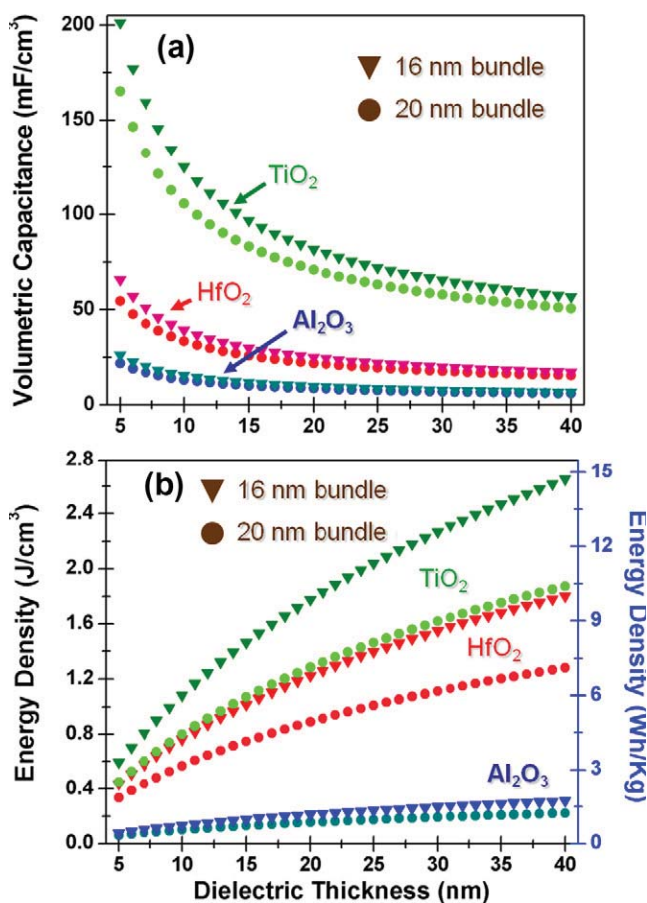


Fig. 5 – (a) Theoretical estimates of the capacitance values of an ideal experimental device with a fixed SWNT bundle diameter (16, 20 nm) and a varying dielectric thickness and type (Al_2O_3 , HfO_2 , and TiO_2 , 5–40 nm), (b) energy density, plotted in both J/cm^3 and Wh/kg , based on data presented in panel a and data shown in SI. Details of the modeling approach are available in the SI.

understand the potential of this energy storage material we performed calculations to predict the volumetric capacitance and energy density (Fig. 5a and b) for these SWNT dielectric capacitor architectures (details in supplementary information SI). This modeling approach allows us to make systematic comparisons between the capacitance and energy density performance of capacitors fabricated with identical structure as studied in experiments, but with varying high- k dielectric coatings and thicknesses. For a 15 nm thick Al_2O_3 dielectric layer, the calculated capacitance is $\sim 11 \text{ mF/cm}^3$, near the value of 23 mF/cm^3 observed experimentally. This minor discrepancy is within the range of experimental variability in factors including bundle diameter measurements, SWNT density estimates, doping effects, local coating structure, and the effect of lowered available surface area due to the criss-crossing of bundles of tubes. Nonetheless, this validates the concept that the measured capacitance values are generally in correspondence with that obtained in calculations, allowing us to further utilize the modeling approach to better understand what promise these materials have with optimized parameters. Our use of Al_2O_3 as a dielectric (as noted previously) is rooted in the notion that Al_2O_3 ALD chemistry is one of the most straight-forward for such a proof-of-principle device design. Although the performance that we obtained with Al_2O_3 dielectrics bridges the performance range between a capacitor and a supercapacitor [8], we demonstrate with calculations that modification of only the dielectric material can yield device performance consistent with that of a supercapacitor, and hence we coin this as a supercapacitor architecture. Using other dielectrics that can be coated with ALD (TiO_2 and HfO_2 [22]), significant capacitance enhancements can be obtained versus Al_2O_3 ($C_{\text{max}} \sim 25 \text{ mF/cm}^3$), with C_{max} up to 0.2 F/cm^3 . In addition, by utilizing experimentally measured breakdown voltages for ALD coated films of Al_2O_3 ($\sim 0.6 \text{ V/nm}$) [23], TiO_2 ($\sim 0.6 \text{ V/nm}$) [24], and HfO_2 ($\sim 0.9 \text{ V/nm}$) [25], the energy density is calculated in Fig. 4b from $E = 1/2 CV_{\text{max}}^2$. This is plotted in both J/cm^3 and Wh/kg(carbon) [26] to aid interpretation based on conventional units. Maximum predicted energy densities with conformal TiO_2 dielectrics approach 15 Wh/kg , comparable to a “good” EDLC device. This enhancement over Al_2O_3 is based on the enhanced dielectric constant in TiO_2 that yields greater volumetric capacitance and also the breakdown voltage that scales as the square of the thickness. Additionally, the SWNT materials are known to be highly conductive [27–29] and capable of supporting current densities of 10^9 A/cm^2 (up to three orders of magnitude higher than Cu) [30], meaning that this device architecture provides an excellent template for high power density applications (in the same framework of a classical solid-state capacitor) while still providing a high energy density. Compared to EDLCs, which offer inferior power density compared to classical capacitors, but greater energy density, this device design supports both high power that is expected from a solid-state capacitor architecture and high energy density that can ultimately be tuned by varying the physical parameters of the system (i.e. dielectric thickness, VA-SWNT material properties). Furthermore, the energy density of these supercapacitor architectures can be enhanced by systematic variations to physical parameters

of the VA-SWNT material, such as bundle density, SWNT diameter, and SWNT bundle diameter. Such variations can yield enhancements to the energy density by more than an order of magnitude compared to that shown in Fig. 5 (supplementary information supporting info), which represents an exciting route toward high power density and high energy density solid state energy storage materials. Furthermore, the benefit of these materials in their operation with higher response rates, the use of lightweight electrode materials compatible with high specific energy and power densities, and the versatility associated with solid-state dielectric layers makes this an attractive material for both on-chip and grid-scale energy storage at a time when energy systems will play a crucial role in the future of our modern society.

4. Conclusions

In this study, we demonstrate the experimental design of a solid-state dielectric capacitor with performance commensurate to that of a supercapacitor fabricated utilizing a template made of self-assembled VA-SWNTs. Utilizing ALD as a technique to uniformly coat this VA-SWNT template with dielectric (Al_2O_3) and counter-electrode (Al-ZnO) materials, we demonstrate performance of this energy storage architecture commensurate with theoretical estimates. Furthermore, we calculate the expected performance from the same VA-SWNT material architecture utilizing other high- k dielectrics, and demonstrate the prospect of these devices architectures for high energy density and high power density solid-state energy storage. We envision this energy storage material concept, with proper optimization of the physical characteristics of the VA-SWNT templates as well as optimized materials and material coating techniques, to yield a superior class of materials for solid-state energy storage. Such materials would combine both high energy and power density and be capable of integration into multifunctional applications that would take advantage of the load-bearing nature of the device. We further foresee useful routes in combining such a device architecture with printing methods [31] to support ultra-lightweight energy storage and small footprint power conditioning that can be assembled directly onto microchips or flexible device platforms.

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Appendix A. Supplementary data

Supplementary data associated with this article can be found, in the online version, at doi:10.1016/j.carbon.2011.07.011.

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