High density Ru nanocrystal deposition for nonvolatile memory applications

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(Received 21 February 2007; accepted 11 April 2007; published online 21 June 2007)

Arrays of Ru nanocrystals 1–4 nm in diameter are deposited via a hybrid chemical vapor deposition/atomic layer deposition reaction. The nanocrystal density is found to depend sensitively on the nucleating surface. A maximum density of $(7-8)\times10^{12}$ cm^{-2} is achieved on Al_2O_3. Incorporation of these nanocrystals in floating-gate memory cells results in *C-V* curves that exhibit large, counterclockwise hysteresis. Leakage current analysis reveals Coulomb blockade phenomena, Frenkel-Poole emission, and space-charge-limited conduction. This analysis allows for the determination of nanocrystal size and connectivity. Charge storage converges to approximately 50% of the maximum value after two days. The corresponding loss mechanisms are discussed. © *2007 American Institute of Physics*. [DOI: 10.1063/1.2740351]

I. INTRODUCTION

The floating-gate memory concept has proven to be a crucial component in nonvolatile electronic storage devices. Floating gates composed of discrete nanocrystals as opposed to continuous thin films are of particular interest. Discrete nanocrystal devices offer smaller operating voltages, faster write/erase speeds, and more robust endurance characteristics than their continuous counterparts.[1] A critical consideration in the fabrication of these memory cells is the ability to maximize the spatial density and minimize the size distribution of the nanocrystals. A large spatial density optimizes the charge storing capability of the floating layer, while a high degree of size uniformity ensures reproducible storage characteristics.

Nanocrystal deposition has been achieved using a variety of methods with varying degrees of success. Physical techniques such as pulsed laser deposition and thermally induced processes such as implanted ion self-organization and thin film agglomeration have been employed in nanocrystal fabrication.[2–4] Chemical methods including spin coating of metallic colloids, chemical vapor deposition (CVD), and atomic layer deposition (ALD) have also been investigated.[5–7] Of these methods, ALD and CVD are probably the most promising for industrial applications because they are scalable gas-phase techniques that offer exceptional controllability and conformality over three dimensional structures.

Semiconducting and metallic nanocrystals have been investigated for memory applications. Both materials exhibit promising storage characteristics, but metallic nanocrystals are considered to be more advantageous. They offer the possibility of lower power consumption, better size scalability, improved endurance characteristics, and device optimization through work function engineering.[8,9] Ruthenium (Ru) is particularly well suited for this purpose. As a noble metal, it exhibits high chemical and thermal stability and does not readily migrate or diffuse. These are essential properties needed to ensure device robustness and operational longevity. Furthermore, the high work function of ruthenium (4.7 eV) allows for the creation of electron wells with high barriers, which gives rise to better retention and charging characteristics. Here, we investigate the deposition behavior and memory properties of densely packed Ru nanocrystals deposited by a CVD/ALD hybrid reaction.

II. EXPERIMENT

Ruthenium nanocrystals are deposited using the ruthenium precursor[10] bis(N,N'-di-tert-butylacetamidinato) ruthenium(II) dicarbonyl [Ru(^{t}Bu-Me-amd)$_2$(CO)$_2$] and ammonia (NH_3) at a substrate temperature of 300 °C. This reaction exhibits a CVD component involving thermal decomposition of the amidinate and an ALD component involving increased reactivity and a saturated growth rate during NH_3 exposure. Under optimized conditions, the growth rate of ruthenium films using this reaction is 0.15 nm/cycle.[11,12]

The inherent nucleation inhomogeneity associated with this reaction is exploited to produce electrically isolated nanocrystals. An important point to note is that the degree of inhomogeneity is highly dependent on the nucleating surface. Conventional memory cells use SiO_2 as the tunnel dielectric. In fact, Ru nanocrystal deposition has already been achieved on this surface with ALD.[7] However, the density of nucleation sites on SiO_2 is relatively low, resulting in a low spatial density of nanocrystals. This poor nucleation behavior can be overcome by changing the nucleating surface. This is illustrated in Fig. 1, where Al_2O_3 and SiO_2 surfaces are deposited with 80 cycles of ruthenium.[13] The nucleation site density on Al_2O_3 is large enough to cause the nanocrystals to agglomerate into a continuous thin film, while the nanocrystals on SiO_2 are still well separated. This nucleation behavior

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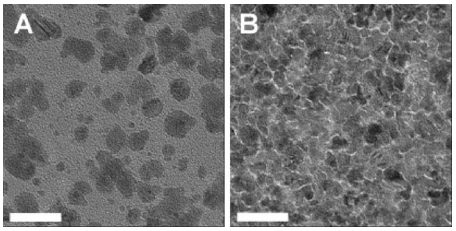

FIG. 1. TEM micrographs illustrating the nucleating ability of different surfaces. 80 cycles of Ru on SiO_2 results in an inhomogeneous surface (a), while the same number of cycles on Al_2O_3 produces a continuous, polycrystalline film (b) (20 nm scale bar).

has been observed in other CVD reactions and is attributed to the variation in hydroxyl density on different surfaces.[6,14,15] The conduction band offset of SiO_2 relative to the conduction band of Si is very large (3.5 eV), so it is still advantageous to incorporate it in the memory cell as a retention enhancement barrier.[16] However, it is also evident that an Al_2O_3 surface should be incorporated to maximize nanocrystal density.

Memory cell gate stack fabrication is carried out on *p*-type Si substrates (14–20 Ω cm) that are coated with 3 nm of thermal SiO_2. To facilitate denser nanocrystal nucleation, 2.5 nm of ALD Al_2O_3 is deposited at 250 °C using trimethylaluminum $[Al(CH_3)_3]$ and water (H_2O) as precursors. This bilayer of Al_2O_3 and SiO_2 serves as the tunnel layer of the device. Varying numbers of ruthenium cycles are then deposited on the Al_2O_3 surface and capped with a 10 nm layer of ALD Al_2O_3, which serves as the control oxide layer of the device. Al_2O_3 has been shown to be an effective barrier against charge injection from the control gate, ensuring proper memory cell operation.[17] It is for this reason that Al_2O_3 is chosen as the control oxide material. Aluminum (50 nm) pads are patterned on the front and back surfaces of the metal-oxide-semiconductor (MOS) structure to serve as the control gate and grounding electrode, respectively. Unless otherwise indicated, the area of the control gate is 1×10^{-4} cm^2. All ensuing electrical measurements are performed under atmospheric conditions at room temperature.

III. RESULTS AND DISCUSSION

Current-voltage (*I-V*) characteristics of memory cells with 0, 5, and 10 cycles of ruthenium are compared in Fig. 2(a). The 0 cycle sample (control sample) exhibits a breakdown field of ~9 MV/cm, which is a reasonable value for the thicknesses of the two oxide layers. The leakage current of this sample prior to breakdown is found to be consistent with Frenkel-Poole (FP) emission [Fig. 2(b)]. In FP emission, the current density is expressed as

$$J_{\mathrm{FP}} = cE \exp\left(\frac{q\sqrt{qE/\pi\varepsilon} - \phi q}{k_B T}\right), \tag{1}$$

where E is the electric field in the insulator, ε is the electric permittivity of the insulator, q is the electric charge, k_B is the Boltzmann constant, T is the temperature, and c is a trap-dependent proportionality constant. The energy ϕq is the depth of FP traps in the insulator relative to the conduction band minimum of the insulator. Observation of FP emission is consistent with previous work that has identified it as the

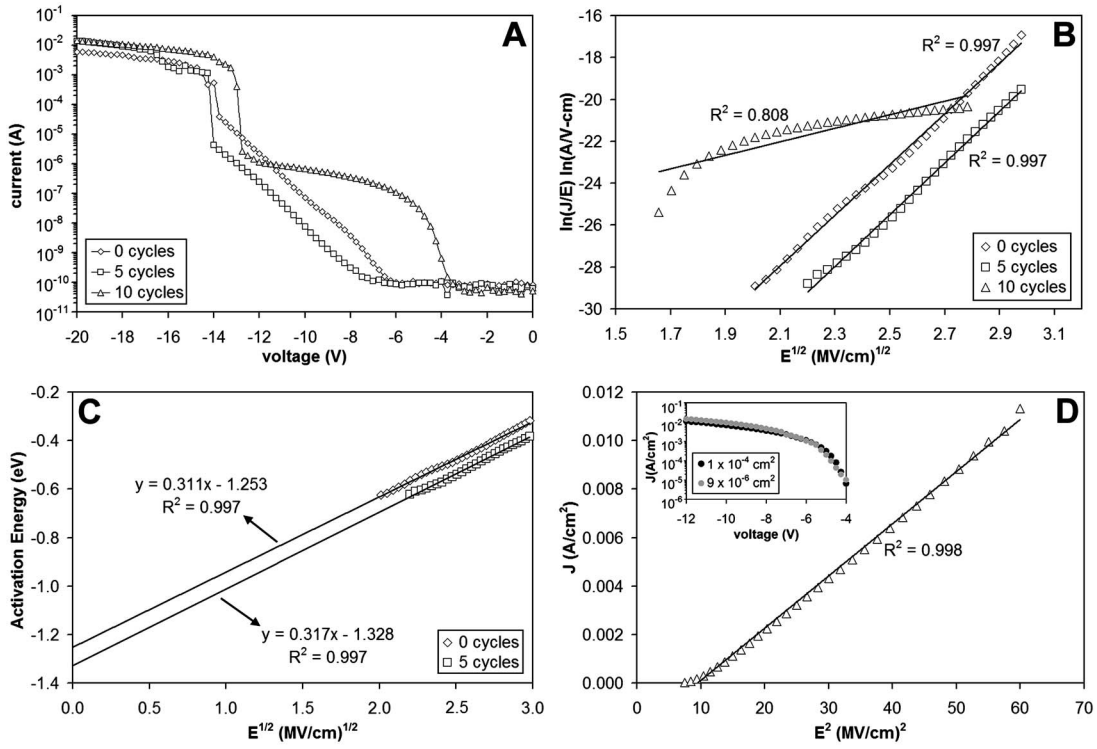

FIG. 2. Leakage properties of the MOS structures. (a) *I-V* characteristics comparing Ru cycle number. (b) Linear behavior on the Frenkel-Poole plot corresponds to FP emission. (c) Activation energy extrapolation from the 0 and 5 cycle samples. (d) The 10 cycle sample exhibits linear behavior on the SCLC plot. The inset illustrates that the leakage in the 10 cycle sample is not affected by changing the area of the gate from 1×10^{-4} to 9×10^{-6} cm^2. (R^2 is the deviation from the linear fits.)

dominant leakage mechanism in Al_2O_3 films.[18] The field-dependent effective activation energy $E_{act}=q\sqrt{qE/\pi\varepsilon}-\phi q$ is plotted from the *I-V* data and used to extrapolate a value of $\phi q=-1.25$ eV [Fig. 2(c)]. This value has been previously reported as the trap depth in Al_2O_3 and is further confirmation that FP emission is the dominant leakage mechanism in the insulator.[19]

Two-probe measurements reveal that the sample with 5 cycles of ruthenium remains insulating to lateral current flow in the plane of the array. This is an indication that the nanocrystals are electrically isolated with a density below the percolation threshold. As in the control sample, FP emission is the dominant leakage mechanism through the MOS structure [Fig. 2(b)]. The breakdown field is also similar to that of the control sample, but the leakage current is notably lower [Fig. 2(a)]. This is attributed to the Coulomb blockade charging effect.[20] When an electron enters the nanocrystal, the charge resists injection of additional electrons, and hence decreases the leakage current. At room temperature, this charging effect is only observable in small, electrically isolated systems. Observation of this effect therefore signifies the presence of discrete Ru nanocrystals. The FP trap depth in the 5 cycle sample is found to be $\phi q=-1.33$ eV [Fig. 2(c)]. Relative to the trap depth in the control sample, this corresponds to an energy decrease of −80 meV. The charging energy of nanocrystals with a capacitance C and a diameter d can be calculated from the relation $U=q^2/2C=q^2/4\pi\varepsilon d$. Using this expression in conjunction with the fact that the nanocrystals are encased in ALD Al_2O_3 ($\varepsilon\approx 8\varepsilon_o$), the −80 meV energy change can be found to correspond to a nanocrystal diameter of 2–3 nm. Transmission electron microscopy (TEM) of these nanocrystals reveals the diameter distribution to be 1–4 nm, in good agreement with the Coulomb charging analysis [Fig. 3(a)].

When the ruthenium cycle number is doubled to 10 cycles, two-probe analysis reveals measurable, lateral conduction through the array, suggesting that the nanocrystals are connected. Analysis of the leakage current through the MOS structure complements this observation by providing additional connectivity information. The leakage current exhibits a nonlinear dependence on the square root of the field, signifying that FP emission is no longer the dominant conduction mechanism [Fig. 2(b)]. Also, the leakage increases above the noise of the measurement system at much lower voltages [Fig. 2(a)]. This behavior is independent of the control gate area and is therefore not the result of inhomogeneously distributed defects in the oxide layers [Fig. 2(d) inset]. It is rather due to a more fundamental change in the dominant transport mechanism through the insulator. We propose that the earlier onset of leakage is the result of nanocrystals becoming connected, effectively forming a continuous metallic sheet. This eliminates the previously observed charging effects and provides an ample number of energetically favorable electronic states to facilitate more efficient transport through the oxide. The dominant leakage mechanism now appears to be space-charge-limited conduction (SCLC) [Fig. 2(d)]. SCLC has a quadratic dependence on the electric field and can result when transport is limited by the capture of carriers in the dielectric.[21] This is further affirmation that the nanocrystals are indeed connected. Leakage current is no longer limited by field-assisted FP trap hopping but rather by the large number of states provided by the continuous metal sheet. Another possibility is that the transport is limited by charge accumulation at the Al_2O_3/SiO_2 interface in the tunnel layer. This has been found to cause SCLC in other multilayer oxides.[18,22] However, since it is not observed in the other samples, the ruthenium sheet seems to be the more likely cause of SCLC in this case. These interpretations are validated by TEM analysis, which reveals the Ru nanocrystals to be physically connected after 10 cycles [Fig. 3(b)]. For this reason, 5 cycles of ruthenium are determined to be the optimized number of cycles to produce nanocrystals that are both spatially dense and electrically isolated. The array after 5 cycles is determined by TEM to have a strikingly high density of $(7-8)\times 10^{12}$ cm^{-2}. This is almost an order of magnitude higher than previously reported Ru nanocrystal densities and at least twice the density reported for other types of nanocrystals.[5,7,23,24]

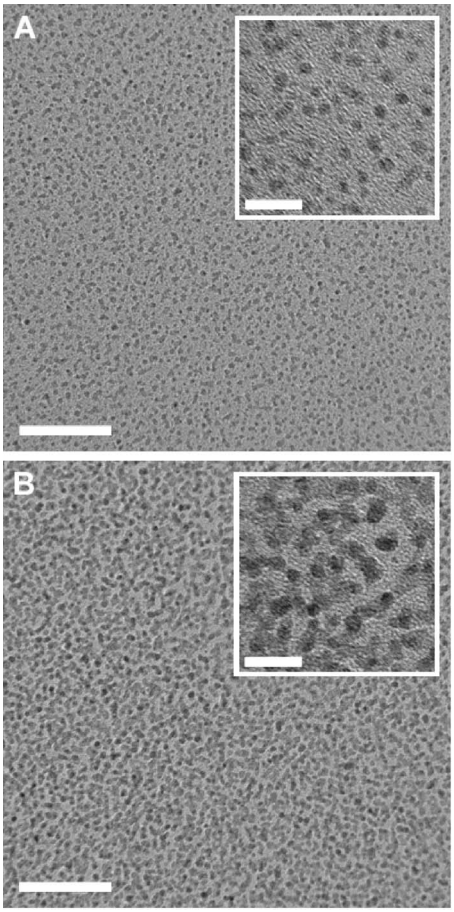

FIG. 3. TEM micrographs illustrating different amounts of Ru deposition on Al_2O_3. 5 cycles of deposition produce nanocrystals that are physically separated (a), while 10 cycles result in nanocrystals that are connected (b). The insets are higher magnification images (40 nm scale bar, inset: 10 nm scale bar).

High frequency (1 MHz) capacitance-voltage (*C-V*) analysis is used to investigate the memory properties of the 0 and 5 cycle samples. As expected, the 0 cycle sample exhibits negligible hysteresis (≤100 mV), indicating that only a very small amount of charge is stored in the dielectric. The

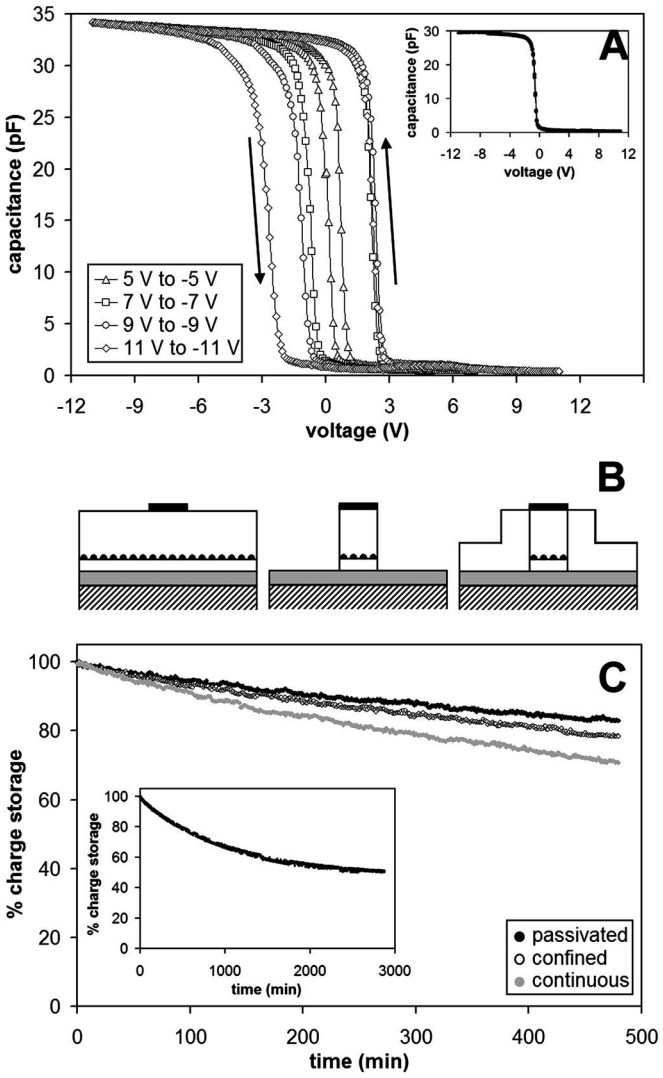

FIG. 4. Capacitance analysis of the MOS structures. (a) *C-V* curves of cells with embedded nanocrystals (5 cycles) exhibit counterclockwise hysteresis, while cells without nanocrystals (0 cycle) show negligible hysteresis over the same voltage ranges (inset). (b) Configuration of memory cells with a continuous nanocrystal array (left), confined array (middle), and a passivated array (right). (c) Retention characteristics improve when the continuous array is confined under the gate and the sidewalls are passivated with insulating material to minimize leakage. The inset illustrates the charge loss of a passivated cell during a longer stress time (write: 7 V for 30 s, read: 1 V).

flatband voltage is also constant through multiple voltage sweeps of different magnitudes, indicating the absence of injected or mobile charge [Fig. 4(a) inset]. This behavior is dramatically altered when Ru nanocrystals are embedded in the gate stack. *C-V* curves from the 5 cycle sample are characterized by the existence of prominent memory windows centered at low voltages [Fig. 4(a)]. This window initially appears at small sweep ranges and continues to increase in width with larger sweeps. A maximum flatband voltage shift of 5.4 V is attained at a 22 V sweep (11 V $\rightarrow -11$ V $\rightarrow$ 11 V). The hysteresis is counterclockwise, indicating that electrons are being injected from the inverted *p*-type Si surface at positive voltages and back into the Si at negative voltages. When compared to the *C-V* characteristics of the 0 cycle sample, it can be concluded that the hysteresis results from the presence of the nanocrystals. The amount of trapped charge can be estimated by the relation $N=(C_{FB}\Delta V_{FB})/q$, where C_{FB} is the flatband capacitance and ΔV_{FB} is the flatband voltage shift. The maximum value of ΔV_{FB} corresponds to a charge density of $8\times10^{12}-1\times10^{13}$ cm^{-2}. The number of trapped charges is therefore roughly equal to the number of nanocrystals. This can be interpreted as another manifestation of the Coulomb blockade effect and suggests that the charge is being stored in the nanocrystals as opposed to states at the oxide/nanocrystal interface.[25]

Charge retention and the mechanisms of charge loss in the nanocrystal array are studied by modifying the geometry of the memory cells [Fig. 4(b)]. The nanocrystals are fully charged at a control gate voltage of 7 V for 30 s, and the subsequent charge loss is measured at a constant bias of 1 V. Charge loss of the continuous nanocrystal array after 1000 s of stress time is 2%, which suggests good retention properties, and is similar to the loss rate of other nanocrystal memory devices.[2,26,27] Phosphoric acid is then used to selectively etch the Al_2O_3 and embedded nanocrystals bordering the control gate area. This produces a confined configuration, where the nanocrystal array in the region underneath the gate is isolated from neighboring nanocrystals outside this region. This confined geometry results in an 8% increase in retention after 8 h, which suggests lateral charge loss as a prevalent mechanism when the array is continuous.[28] Since these measurements are made under atmospheric conditions, the confined geometry is susceptible to leakage at the sidewalls created by the etch. Therefore, further retention improvement is attained by passivating the sidewalls with a 5 nm layer of Al_2O_3, resulting in an additional 4% improvement after 8 h. These results are illustrated in Fig. 4(c), where each curve represents the average of three measurements. The standard deviations associated with these measurements are 2.7% for the continuous array, 3.1% for the confined array, and 1.9% for the passivated array. As expected, minimum dispersion in the decay profile is achieved when the nanocrystals are fully passivated on all sides. After a 48 h period, charge loss in the passivated cells is observed to stabilize and converge to 50% [Fig. 4(c) inset]. Since alternate leakage pathways have been reduced or eliminated in passivated cells, emission of electrons back into the silicon is the most likely loss mechanism.

IV. CONCLUSION

In summary, high density ruthenium nanocrystal arrays have been deposited via a CVD/ALD hybrid reaction by utilizing the relatively high nucleating ability of Al_2O_3. Analysis of the leakage current through the gate stack was used to identify and characterize Coulomb blockade phenomena and to reliably estimate nanocrystal size. Leakage current analysis was also used to differentiate electrically isolated nanocrystals from connected nanocrystals, which facilitated optimization of the processing parameters. Capacitance analysis of nanocrystal-embedded gate stacks revealed the existence of large memory windows centered at low voltages. The memory retention properties were determined to be relatively robust. Charge loss was reduced by making smaller devices with smaller lateral conduction losses, and further reduced

by encapsulating the devices in passivating material. Since the deposition technique is easily scalable, it is feasible that further engineering can be employed to optimize device performance and produce memory cells with potentially useful applications.

ACKNOWLEDGMENT

A portion of the work presented here was carried out at the Center for Nanoscale Systems at Harvard University.

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