# Atomic layer deposition of insulating nitride interfacial layers for germanium metal oxide semiconductor field effect transistors with high-$\kappa$ oxide/tungsten nitride gate stacks

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Atomic layer deposition (ALD) was used to deposit passivating interfacial nitride layers between Ge and high-$\kappa$ oxides. High-$\kappa$ oxides on Ge surfaces passivated by ultrathin (1–2 nm) ALD $Hf_3N_4$ or AlN layers exhibited well-behaved *C-V* characteristics with an equivalent oxide thickness as low as 0.8 nm, no significant flatband voltage shifts, and midgap density of interface states values of $2\times10^{12}$ $cm^{-1}$ $eV^{-1}$. Functional *n*-channel and *p*-channel Ge field effect transistors with nitride interlayer/high-$\kappa$ oxide/metal gate stacks are demonstrated. © *2007 American Institute of Physics*. [DOI: 10.1063/1.2741609]

With the advancement of deposition techniques for thin, high-permittivity (high-$\kappa$) dielectric films, significant progress has recently been made towards integrating high-$\kappa$ dielectric materials into conventional metal oxide semiconductor (MOS) processes.[1] The incorporation of *deposited* gate dielectrics into gate stacks provides an opportunity to consider high mobility semiconductors such as germanium for future MOS devices. The absence of a chemically stable thermal oxide has been the main obstacle hindering the use of Ge channels in MOS devices. Deposited high-$\kappa$ gate dielectrics can possibly avoid this problem. A key issue for integrating deposited high-$\kappa$ dielectrics with Ge is the formation of a high quality Ge/dielectric interface.

High-$\kappa$ dielectrics deposited directly on wet-cleaned (dilute HF or HCl) Ge surfaces generally exhibit high density of interface charge traps and very poor leakage current characteristics.[2] One solution to this problem involves growing a thin germanium oxynitride ($GeO_xN_y$) interfacial layer by rapid thermal nitridation followed by deposition of a high-$\kappa$ dielectric.[3–5] It has been shown that $GeO_xN_y$ interlayers provide a stable and smooth interface with improved electrical properties. Reported shortcomings of the oxynitride passivation method include large negative flatband voltage shift and very low electron mobility for *n*-channel MOS field effect transistors (MOSFETs).[2] While nitridation of germanium results in a reasonable quality native insulator, this approach may be limited by the fundamentally poor material and electrical properties of $GeO_x$. Consequently, alternative deposition-based and surface-treatment methods [AlN,[6] $PH_3$,[6] and $SiH_4$[7]] have been proposed.

In this letter, we show that atomic layer deposition (ALD) of ultrathin insulating nitride layers such as AlN and $Hf_3N_4$[8] can effectively passivate the Ge surface and produce functional *n*-channel and *p*-channel Ge MOSFETs with reasonable mobility values. AlN ($\kappa\sim9$) and $Hf_3N_4$ ($\kappa\sim20$) have higher $\kappa$ values than $GeO_xN_y$ ($\kappa\sim6-7$) and depositions of AlN and $Hf_3N_4$ do not require high temperature processes that can be detrimental to the device performance.

The Ge substrates used for device fabrication were Ga-doped *p*-type (100) substrates with resistivity of 0.2–0.4 Ω cm and Sb-doped *n*-type (100) substrates with resistivity of 0.025–0.04 Ω cm. The Ge substrates were immersed in dilute HF solution (10%) for 5 min to remove the native oxide and then rinsed in de-ionized water for 30 s.[4] Immediately after wet cleaning, the substrates were transferred into a custom-built, hot-wall ALD reactor. Tris[dimethylamido] aluminum and tetrakis [ethylmethylamido] hafnium precursors were used for AlN and $Hf_3N_4$, respectively. Both of the precursors were vaporized at approximately 80 °C and delivered to the deposition zone by a $N_2$ carrier stream. The deposition temperature for these nitride layers was 200–250 °C and purified $NH_3$ gas was used as a coreactant. *In situ* ALD of high-$\kappa$ oxide films [$HfO_2$,[9] $LaAlO_3$,[10] or $GdScO_3$[11]] immediately followed the deposition of the nitride layers and the gate electrode was also formed *in situ* using ALD WN [Fig. 1(a)]. The samples then underwent rapid thermal annealing at 420 °C for 2–3 min in forming gas (1:10 $H_2$/He mixture at 5 Torr).

For MOS capacitors, Pt was sputtered through a shadow mask to produce pads that served as top contacts as well as etch masks for reactive ion etching of WN. Ge MOSFET

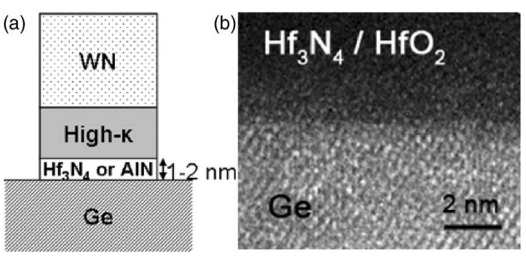


FIG. 1. (a) Schematic diagram of a high-$\kappa$ oxide/WN gate stack with a nitride interlayer (b) Cross-sectional TEM image of $Hf_3N_4/HfO_2$ gate dielectric stack on Ge. There is no evidence of a low-$\kappa$ interlayer formation between Ge and $Hf_3N_4$.

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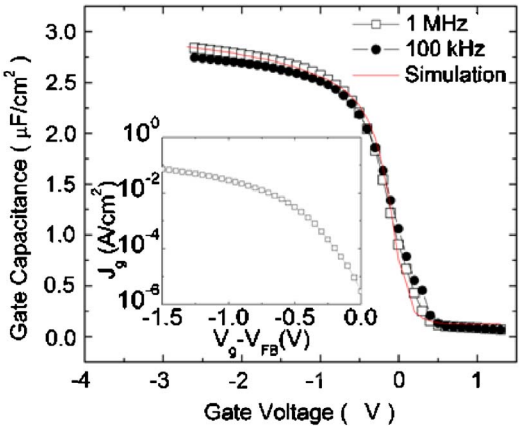


FIG. 2. (Color online) *C-V* curves of a *p*-Ge/$Hf_3N_4$/$HfO_2$/WN MOS capacitor with an EOT of 0.82 nm. Inset shows the corresponding leakage current density curve as a function of $V_g$-$V_{FB}$.

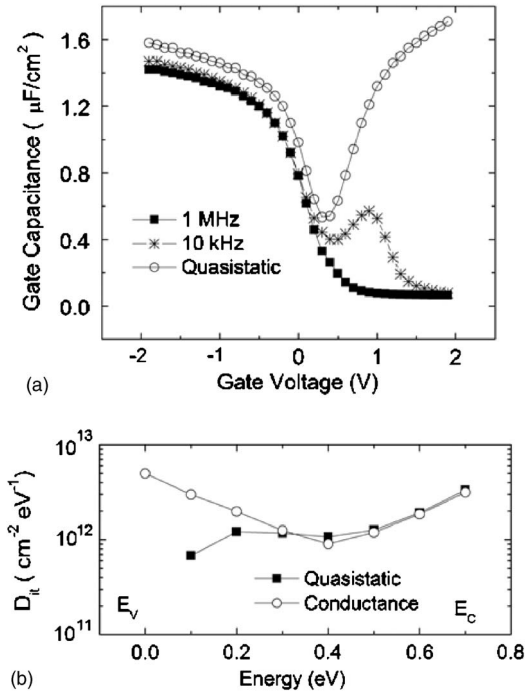


FIG. 3. (a) Quasistatic and high frequency *C-V* curves of a *p*-Ge/$Hf_3N_4$/$GdScO_3$/WN MOS capacitor (b) $D_{it}$ values extracted from the *C-V* curves in (a) compared to those extracted by the frequency dependent conductance method.

devices were fabricated in concentric ring geometry with three different gate lengths, 5, 10, and 20 $\mu$m. The source/drain (S/D) dopant activation conditions were 500 °C, 60 s for *n*-channel devices and 450 °C, 60 s for *p*-channel devices, both in a $N_2$ ambient. The temperature required for acceptable *n*-type dopant activation was determined experimentally. Ti/Al metallization was used for contacts to the source, drain, and gate.

The thickness was linearly proportional to the number of ALD cycles for both AlN and $Hf_3N_4$ deposition processes. The growth rates of the AlN and $Hf_3N_4$ films were 1.5–1.8 Å/cycle with almost zero incubation time, which implies that AlN and $Hf_3N_4$ nucleate on HF-cleaned Ge surfaces very effectively. Compositional analysis of thick AlN and $Hf_3N_4$ films on amorphous carbon substrates by Rutherford backscattering showed that the oxygen and carbon contents are below 1%. Both nitride films were amorphous as deposited according to x-ray diffractometry measurements, and remained amorphous after the S/D activation process.

Cross-sectional transmission electron microscopy (TEM) micrographs [Fig. 1(b)] show no evidence of significant low-$\kappa$ layer ($GeN_x$ or $GeO_xN_y$) formation at the interface during deposition. The root mean square (rms) roughness of either nitride film measured by AFM was below 0.5 nm and was independent of the film thickness for thicknesses greater than 1.5 nm. The rms roughness of wet-cleaned Ge substrate before deposition was 0.2–0.3 nm.

Capacitance-voltage (*C-V*) characteristics of various Ge/[AlN or $Hf_3N_4$]/high-$\kappa$ oxide/WN MOS capacitors were measured at different frequencies. Figure 2 shows 100 kHz and 1 MHz *C-V* curves of a *p*-Ge/$Hf_3N_4$/$HfO_2$/WN MOS capacitor. The total physical thickness of the dielectric was 4 nm and the thickness of the nitride interlayer was approximately 1.5 nm. An equivalent oxide thickness (EOT) of 0.82 nm and flatband voltage of 0.01 V were determined by fitting the measured data with the MISFIT[12] simulation program (including quantum mechanical effects). The measured *C-V* curves showed good agreement with simulation assuming a uniform distribution of hole traps with density of $2.0 \times 10^{12}$ $cm^{-2}$ $eV^{-1}$. There was no significant frequency dispersion and the flatband voltage shift was minimal. Small humps were present in the midgap region for *C-V* curves measured at frequencies lower than 100 kHz, which indicates slowly responding trap states. Some near-interface or bulk charge traps were also present as evidenced by hysteresis in the *C-V* curves. In general, the hysteresis ranged from 0.1 to 0.3 V for these films and was about 0.15 V for the *C-V* curves shown in Fig. 2. The inset in Fig. 2 displays the corresponding leakage current density plot for the accumulation region. The leakage current density is approximately 0.01 A/$cm^2$ at $|V_g - V_{FB}|$ equal to 1.0 V.

To study the properties of the Ge/nitride interface in more detail, we employed two measurement techniques that are generally used to measure interface trap density ($D_{it}$): quasistatic *C-V* and frequency dependent conductance measurements. Figure 3(a) shows quasistatic, 10 kHz, and 1 MHz *C-V* curves for a *p*-Ge/$Hf_3N_4$/$GdScO_3$/WN MOS capacitor. The thicknesses of the $Hf_3N_4$ and $GdScO_3$ layers were approximately 1.5 and 8 nm, respectively. The normal quasistatic *C-V* curve implies reasonably good interface quality. The difference in $C_{MAX}$ for the *C-V* curves in Fig. 3(a) is probably due to the parasitic series resistance. The filled squares in Fig. 3(b) denote $D_{it}$ values extracted from the quasistatic and 1 MHz *C-V* curves.[13] Conductance of the same MOS capacitor was also measured at frequencies ranging from 1 kHz to 1 MHz. $D_{it}$ was extracted from the conductance data and the values are plotted as empty circles in Fig. 3(b).[14] The midgap $D_{it}$ values obtained from the two different methods are in the same range, $1 \times 10^{12}$–$3 \times 10^{12}$ $cm^{-2}$ $eV^{-1}$.

We fabricated *n*-channel and *p*-channel Ge MOSFETs with gate stacks employing AlN and $Hf_3N_4$ interlayers. AlN provided optimum performance for *p*-channel devices while $Hf_3N_4$ provided optimal performance for *n*-channel devices. Figure 4 shows the $I_S$-$V_G$ plots for a *n*-channel device with a $Hf_3N_4$/$GdScO_3$/WN gate stack and a *p*-channel device with an AlN/$LaAlO_3$/WN gate stack. Both devices showed $I_{ON}/I_{OFF}$ ratio of approximately $10^6$ at $V_{DS}$=1.5 V. The threshold voltage of the *n*-channel device was 0.33 V and the inverse subthreshold slope (SS) was 94 mV/decade. The

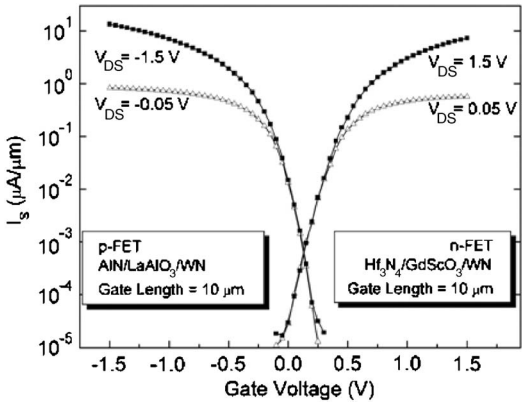


FIG. 4. Source current vs gate voltage for *n*-channel MOSFET with $Hf_3N_4/GdScO_3/WN$ gate stack and *p*-channel MOSFET with $AlN/LaAlO_3/WN$ gate stack. The gate length was 10 $\mu$m for both devices. The current was measured at the source to prevent the characteristics from being affected by drain junction leakage to the substrate.

*p*-channel device had a threshold voltage of −0.04 V and a SS of 81 mV/decade. The following equation was used to estimate the interface state density of the devices:[15]

$$S = (kT/q)\ln 10(1 + C_D/C_i + C_{\mathrm{it}}/C_i), \quad (1)$$

where $C_D$, $C_i$, and $C_{\mathrm{it}}$ are the depletion capacitance, the gate capacitance, and the interface trap capacitance, respectively. This model assumes a uniform distribution of interface traps in the lower half of the band gap for *p*-channel devices and upper half of the band gap for *n*-channel devices. The $D_{\mathrm{it}}$ values extracted by this method are $5.4\times10^{12}$ $\mathrm{cm}^{-2}\,\mathrm{eV}^{-1}$ for the *n*-channel device and $2.2\times10^{12}$ $\mathrm{cm}^{-2}\,\mathrm{eV}^{-1}$ for the *p*-channel device. These values suggest an asymmetrical interface distribution and are similar in magnitude to those obtained from MOS capacitors.

Figure 5 shows the effective electron and hole mobilities extracted from same device $I_S$-$V_G$ [Fig. 4(a)] and split *C*-*V* data. The *p*-channel device shows mobility slightly higher than Si universal but the *n*-channel device shows degraded mobility relative to Si. Prior published work on Ge *n*-channel devices with GeON interlayers suggested that asymmetry in interface trap density (higher density in upper half of bandgap) may be a major contributor to poor *n*-type MOS performance.[16] Similar results have also been observed for early work on Si MOSFETs with $HfO_2/SiON$ dielectric stacks.[17] While the precise mechanism for mobility degradation in Ge *n*-channel devices with ALD nitride interlayers is not completely understood, it is possible that this is an inherent shortcoming of the Ge-nitride interface. It is important to note that *C*-*V* hysteresis for Ge with the nitride interlayers was generally higher by 0.1–0.2 V than on Si when the same high-$\kappa$ oxides were used.[11] This indicates that there are significant charge traps either in the nitride interlayers or at the interface between the nitride interlayers and very thin $GeO_x$ layers that are not completely removed by wet cleaning.[18]

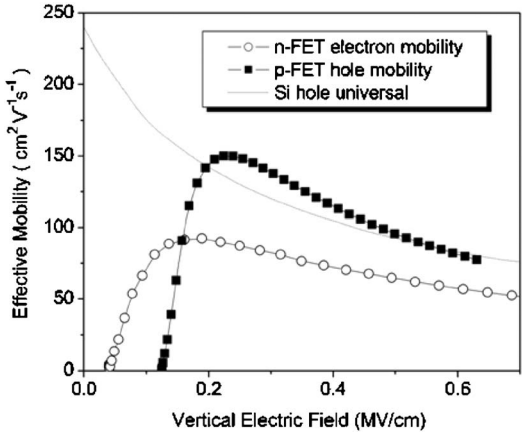


FIG. 5. Effective carrier mobility of *n*-channel and *p*-channel Ge MOSFETs. Mobility was extracted from $I_S$-$V_G$ data shown in Fig. 4 and corresponding split *C*-*V* data.

Although ALD nitride passivation layers still need improvement with regard to interface trap density, this work demonstrates that ALD can be a useful method for depositing very thin passivation layers on Ge surfaces. A recent report[19] suggests that sulfur passivation provides a better interface than nitrogen passivation so ALD of thin metal sulfide layers may offer further improvement. Material flexibility (nitrides, sulfides, phosphides, etc.) and layer-by-layer composition control capability suggest that ALD may play an important role in developing a simple, complementary-MOS-compatible Ge passivation method.

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