Low-temperature atomic-layer-deposition lift-off method for microelectronic and nanoelectronic applications

M. J. Biercuk,[a] D. J. Monsma, and C. M. Marcus
Department of Physics, Harvard University, Cambridge, Massachusetts 02138

J. S. Becker and R. G. Gordon
Department of Chemistry and Chemical Biology, Harvard University, Cambridge, Massachusetts 02138

(Received 2 June 2003; accepted 23 July 2003)

We report a method for depositing patterned dielectric layers with submicron features using atomic layer deposition. The patterned films are superior to sputtered or evaporated films in continuity, smoothness, conformality, and minimum feature size. Films were deposited at 100–150 °C using several different precursors and patterned using either electron-beam or photoresist. The low deposition temperature permits uniform film growth without significant outgassing or hardbaking of resist layers. A lift-off technique presented here gives sharp step edges with edge roughness as low as ~10 nm. We also measure dielectric constants (κ) and breakdown fields for the high-κ materials aluminum oxide (κ~8–9), hafnium oxide (κ~16–19), and zirconium oxide (κ~20–29), grown under similar low temperature conditions. © *2003 American Institute of Physics.*
[DOI: 10.1063/1.1612904]

A variety of applications require thin-film oxides as gate dielectrics, simple insulators, or protective coatings. The push for dielectric layers exhibiting high conformality, uniform stoichiometry and thickness, large breakdown fields, and high dielectric constants has motivated a search for alternatives to SiO_2 and associated deposition techniques.[1–3] An emerging deposition technique that offers relatively precise control of composition, conformality over high-aspect-ratio structures, and thickness control is atomic layer deposition (ALD).[4] ALD is a self-limiting deposition process where separate precursor gases for a target material are sequentially and cyclically dosed into a vacuum chamber under computer control. Substantial work has been invested to develop ALD processes that yield high quality films and use precursor gases that do not chemically damage pre-existing device structures.[5]

Previously, a significant shortcoming of ALD was that, like chemical vapor deposition (CVD), patterning of dielectrics required a *subtractive* process, in which whole layers were deposited, and patterning was done by etching. This limitation arose from the need to use deposition temperatures exceeding 300 °C, which destroyed resist layers or caused them to outgas and disrupt film growth. In precise applications, etch steps are often unacceptable as they can damage other device structures. Moreover, it is difficult to pattern fine features by etching; first, because any subtractive process requires leaving a patch of resist on the substrate the same size as the desired feature, and second, because low energy dielectric etches (which do not damage the device) are generally isotropic, causing feature shape change and undercutting.[3] In contrast, lift-off patterning allows one to cut a ''slit'' in a resist layer and deposit material only where needed. It is therefore desirable to develop lift-off processes for dielectrics similar to those used for metallization. High quality dielectric films patterned by lift-off would be of great value not only in the semiconductor industry, but also in optical applications,[6,7] as catalysts,[8,9] and as protective coatings.[10,11] We note that although polymer resists have been used previously in crudely patterning ALD films for profilometry measurements, actual lift-off lithographic patterning has not been reported to date.[12]

In this letter we demonstrate a process that allows ALD-grown dielectric films to be patterned using lift-off. Examples described in detail are the high-κ materials aluminum oxide (Al_2O_3) and hafnium oxide (HfO_2). The ALD process employed operates at low temperature and uses noncorrosive precursor gases. The patterned films are uniform in thickness with deviations ~1 nm, and are conformal to underlying device structures. ALD lift-off is demonstrated for both photolithography and electron-beam lithography, yielding films with patterned features below 100 nm. We have also measured the dielectric constants and breakdown fields of comparably grown unpatterned films of Al_2O_3, HfO_2, and ZrO_2, finding κ~8.2–9 for Al_2O_3, κ~16.3–18.5 for HfO_2, and κ~20–29 for ZrO_2, at various film thicknesses and measurement temperatures. All films measured exhibit breakdown fields between 5.6 and 9.5 MV/cm, varying with material, film thickness, and measurement temperature (see Table I).

The photolithographic ALD process consisted of the following steps. First, centimeter-scale pieces of a polished Si wafer with 1 μm of thermally grown oxide were cleaved, cleaned (5 min in each of tricholoroethylene, acetone, methanol) and baked for 5 min at 160 °C to drive off solvent residues. Next, Shipley 1813 or 1818 photoresist was spun onto the samples, after which they were baked for 2 min at 120 °C and exposed through a photomask with large features (>10 μm). Patterns were developed using tetramethyl ammonium hydroxide and cleaned for 30 s in 100 W oxygen plasma at 700 mTorr. Thin films were then grown on these samples via

[a]Author to whom correspondence should be addressed; electronic mail: biercuk@physics.harvard.edu

TABLE I. Properties of several high-κ materials grown using the same low-temperature ALD process as used for lift-off, measured at 20 K and room temperature (T_M): breakdown field, $E_{BD}=V_{BD}/d$ (V_{BD} is breakdown voltage, d is film thickness), dielectric constant κ, and charge density at breakdown, $Q_{BD}=CV_{BD}$.

Material	d	T_M	E_{BD}	κ	Q_{BD}
Al_2O_3	2.5 (nm)	RT	8 (MV/cm)	9	6.4 (μC/cm^{-2})
Al_2O_3	10	RT	8.3	8.8	6.5
Al_2O_3	25	RT	8.2	8.2	6.0
Al_2O_3	50	RT	7.6	8.9	6.0
ZrO_2	25	RT	5.6	20	9.9
ZrO_2	100	RT	6	29	15.5
ZrO_2	50	20 K	8.2	29	21
ZrO_2	100	20 K	9.5	26	22
HfO_2	10	RT	6.5	17	9.7
HfO_2	25	RT	7.4	18.5	12
HfO_2	25	20 K	8.4	16.3	12.1

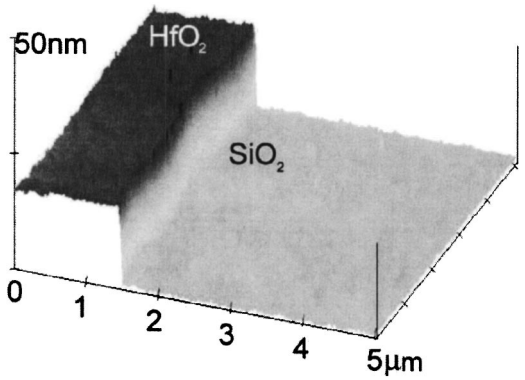

FIG. 1. AFM surface plot of a ~22 nm thick mesa of ALD oxide patterned on a Si/SiO_2 substrate by photolithography shows a well defined and highly vertical step. The waviness seen in the edge is limited by the photolithography. Note the vertical edge profile and edge smoothness.

ALD, as described later. The electron-beam ALD process, used for fabricating fine features, began with similar Si samples, cleaved and cleaned using the same three-solvent rinse followed by a 2 min bake at 180 °C. A bilayer of 200 k poly(methylmethacrylate) (PMMA) and 950k PMMA was spun onto a sample and baked for 15 min at 180 °C for each layer, yielding a total PMMA thickness ~350 nm. Fine-line patterns were written and developed in a solution of isopropanol (75%), methyl isobutyl ketone (24%), and methyl ethyl ketone (1%).

The ALD procedure used for both the photolithographic and electron-beam lift-off processes employed highly reactive metal amide precursors [tetrakis(dimethylamido)hafnium (IV) and H_2O for HfO_2; tetrakis(dimethylamido)zirconium (IV) and H_2O for ZrO_2,[5,13–15] and trimethylaluminum and H_2O for Al_2O_3.[16–18] Samples were placed in a stainless steel tube furnace and heated to 100–150 °C. The cycle of precursors was then started, with nitrogen purges between each step. In order to achieve low-temperature deposition with uniform thickness, the nitrogen purge time needed to be lengthened (from ~5 s, used for the 300 °C process, to ~120 s) to prevent physisorption and to remove unreacted gas-phase precursors. Film thicknesses ranged from 2.5 to 100 nm.

Despite the reduced temperature and lengthened total deposition time, the films appear similar in composition to those grown at higher temperatures, although some important differences exist. First, while surface roughness of these films is typically ~5% of total film thickness for high temperature deposition (>200 °C) it is less than 1% total film thickness for deposition temperatures below 150 °C, except where limited by substrate roughness.[19] Second, x-ray diffraction data indicate that 100-nm-thick films of unpatterned HfO_2 grown at or below 100 °C are completely amorphous while those grown at higher temperatures show some crystallinity (<10% for growth temperature up to 200 °C).[19] Low-temperature grown ZrO_2 films characterized in the same manner show an increase in crystallinity from 10% to 60% as the deposition temperature increases from 100 to 150 °C.[19] It is worth noting that amorphous dielectric films are desirable for applications as gate dielectrics due to their smoothness and high breakdown fields compared to polycrystalline films.[20,21]

Following the growth step, the lift-off procedure was carried out by immersing samples in acetone for times ranging from 10 min to 2 h. To allow the acetone to penetrate the conformal dielectric layer and attack the resist below, it was necessary to manually scratch the surface of the film. While still immersed in acetone, ~1 s pulses from an ultrasonic bath were used to dislodge remaining sections of resist.

Atomic force microscope images in Fig. 1 show that the resulting patterned films have surface roughness comparable to that of the SiO_2 substrate (~1 nm), and sharp step edges. Deviation of the edge from a straight line is limited by the photolithography and not film deposition or lift-off. This was verified by examining metal lines deposited in similar patterns, as shown in Fig. 4. Micrographs of patterned ALD films on SiO_2 [Figs. 1(a) and 2(a)] show edge roughness ~10 nm for electron-beam patterning and ~100 nm edge roughness for photolithographic patterning [Figs. 1(b) and 2(b)].

Figure 3 shows a scanning electron microscopy (SEM) image of a device geometry featuring lines of dielectric pat-

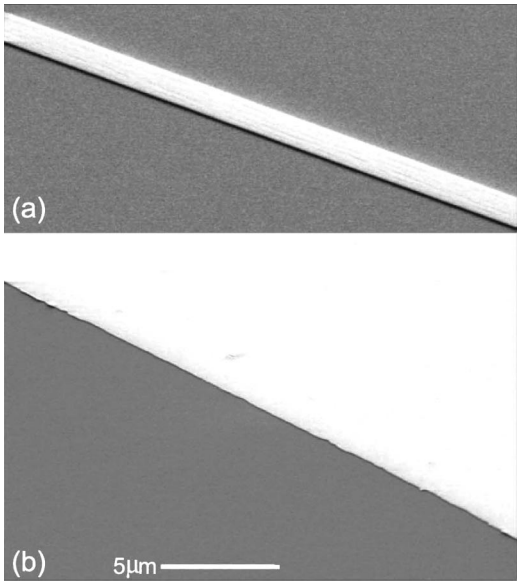

FIG. 2. Scanning electron micrograph showing the smooth edge profiles of ALD patterned via (a) electron-beam lithography and (b) photolithography. Surface roughness was ~1 nm as analyzed by AFM (shadows result from high-angle imaging).

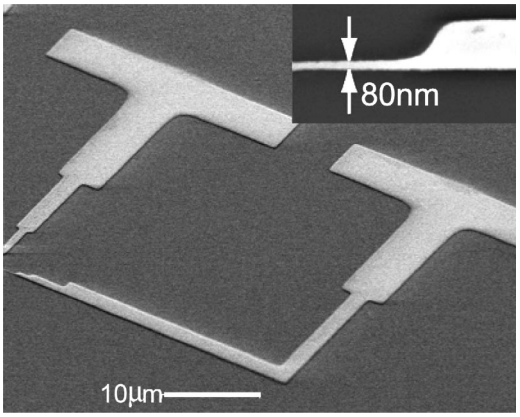

FIG. 3. SEM image of 15-nm-thick HfO_2 on Si/SiO_2, patterned by electron-beam lithography. Device critical dimensions ~80 nm as measured using the SEM. Inset: region of the device showing smallest features.

terned via electron-beam lithography, with smallest dimensions below 100 nm. We have also fabricated complicated multilayer device geometries in which metallic layers are partially coated with patterned ALD films, followed by patterned metallic overlayers. SEM analysis shows (Fig. 4) that patterned ALD films running over metallic lines are highly conformal around the metal line edge and at the metal-substrate interface.

The dielectric constants and breakdown voltages of unpatterned dielectric films grown by low-temperature ALD as described earlier were measured as follows. Films of Al_2O_3, HfO_2, and ZrO_2 were grown on $Si–SiO_2$ substrates with 20 nm Ti+50 nm Pt electrodes deposited by electron-beam evaporation. ALD films were deposited at 150 °C and showed good adhesion to the Pt underlayer. Subsequently 50 nm Pt was evaporated through a shadow mask to form a top electrode of dimension ~200 μm×200 μm. These trilayer structures formed parallel-plate capacitors, which were characterized in a vacuum probe station at 20 K and room temperature. A 1 kΩ resistor was placed in series with these test devices, and digital lock-ins were used to measure the voltage drops across both the resistor and the test device. The circuit was voltage biased using a function generator with an excitation of ~100 mV at 1 kHz. Voltages across the resistor

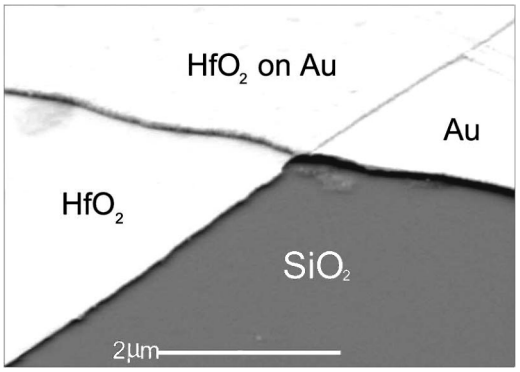

FIG. 4. Multilayer structure (30 nm ALD oxide and 70 nm Ti/Au, both patterned using photolithographic lift-off) showing high conformality of the ALD around the edge of the Ti/Au.

(V_R) and test device (V_C) were used to measure the capacitance of the test device, $C=V_R(2\pi fRV_C)^{-1}$ and, hence, the dielectric constant of the film, $\kappa=Cd/A\epsilon_0$ (A is the device area; d is the film thickness). Dielectric constants κ~20–29 are found for ZrO_2, κ~16–19 for HfO_2, and κ~8–9 for Al_2O_3 (see Table I). Breakdown fields $E_{BD}=V_{BD}/d$ were found by applying an increasing dc bias until the onset of a large leakage current was observed at V_{BD}. Values obtained are in the range E_{BD}~6–9 MV/cm for all three materials, approaching the breakdown fields for high-quality SiO_2 films. Resulting values for dielectric constants, breakdown fields, and calculated charge densities presented in Table I for varying thicknesses and measurement temperatures of the materials. It is interesting to note that the values we obtain for breakdown fields in these devices are two to three times higher than those previously reported in the literature for HfO_2 and ZrO_2.[22–24] We believe the difference is due to the low-temperature growth process, which produces amorphous films.

This work was supported by funding from the National Science Foundation through the Harvard MRSEC, NSF-DMR-0213805 and NSF-CTS 0236584, and the Army Research Office, under DAAD19-02-1-0039 and DAAD19-02-1-0191. M.J.B. acknowledges support from a NSF Graduate Research Fellowship.

[1] G. D. Wilk, R. M. Wallace, and J. M. Anthony, J. Appl. Phys. **89**, 5243 (2001).
[2] M. Gutsche, H. Seidl, J. Leutzen, A. Birner, T. Hecht, S. Jakschik, M. Kerber, M. Leonhardt, P. Moll, T. Pompl, H. Reisinger, S. Rongen, A. Saenger, U. Schroeder, B. Sell, A. Wahl, and D. Schumann, Tech. Dig. - Int. Electron Devices Meet. **2001**, 18.6.1 (2001).
[3] M. Quirk and J. Serda, *Semiconductor Manufacturing Technology* (Prentice-Hall, Englewood Cliffs, NJ, 2001).
[4] M. Leskela and M. Ritala, J. Phys. IV **9-Pr8**, 837 (1999).
[5] D. M. Hausmann, E. Kim, J. S. Becker, and R. G. Gordon, Chem. Mater. **14**, 4350 (2002).
[6] A. J. Waldorf, J. A. Dobrowolski, B. T. Sullican, and L. M. Plante, Appl. Opt. **32**, 5583 (1993).
[7] C. Urlacher and J. Mugnier, J. Raman Spectrosc. **27**, 785 (1996).
[8] J. Nawrocki, M. P. Rigney, A. McGormick, and P. W. Carr, J. Chromatogr. A **657**, 229 (1988).
[9] K. Asakura, M. Aoki, and Y. Iwasawa, Catal. Lett. **1**, 394 (1988).
[10] H. Ibegazene, S. Aplerine, and C. Diot, J. Mater. Sci. **30**, 938 (1995).
[11] J. Wang, H. Li, and R. Stevens, J. Mater. Sci. **27**, 5397 (1992).
[12] J. W. Elam and S. M. George, Chem. Mater. **15**, 1020 (2003).
[13] R. G. Gordon, D. Hausmann, E. Kim, and J. Shepard, Chem. Vap. Deposition **9**, 73 (2003).
[14] R. G. Gordon, J. Becker, D. Hausmann, and S. Suh, Mater. Res. Soc. Symp. Proc. **670**, K2.4/1 (2002).
[15] R. G. Gordon, J. Becker, D. Hausmann, and S. Suh, Chem. Mater. **13**, 2463 (2001).
[16] A. W. Ott, J. W. Klaus, J. M. Johnson, and S. M. George, Thin Solid Films **292**, 135 (1997).
[17] R. Matero, A. Rahtu, M. Ritala, M. Leskelä, and T. Sajavaara, Thin Solid Films **368**, 1 (2000).
[18] A. Rahtu, T. Alaranta, and M. Ritala, Langmuir **17**, 6506 (2001).
[19] D. M. Hausmann and R. G. Gordon, J. Cryst. Growth **249**, 251 (2003).
[20] P. Balk, J. Non-Cryst. Solids **187**, 1 (1995).
[21] K. Kukli, J. Ihanus, M. Ritala, and M. Leskela, J. Electrochem. Soc. **144**, 300 (1997).
[22] J. McPherson, J. Kim, A. Shanware, H. Mogul, and J. Rodriguez, Tech. Dig. - Int. Electron Devices Meet. **2002** (2002).
[23] T. Ma, Solid-State IC Technology Conference Proceedings (2001), p. 297.
[24] L. Kang, B. H. Lee, W. J. Qi, Y. Jeon, R. Nieh, S. Gopalan, K. Onishi, and J. C. Lee, IEEE Electron Device Lett. **21**, 181 (2000).