ALD high-k and higher-k integration on GaAs

Ozhan Koybasi [1)], Min Xu [1)], Yiqun Liu [2)], Jun-Jieh Wang [2)],
Roy G. Gordon [2)], and Peide D. Ye [1)*]

[1)] *School of Electrical and Computer Engineering, Purdue University, West Lafayette, Indiana, U.S.A.*
[2)] *Department of Chemistry and Chemical Biology, Harvard University, Cambridge, Massachusetts, U.S.A.*
**Email: yep@purdue.edu*

Silicon-based CMOS devices with traditional structures are approaching fundamental physical limits. Researchers are looking for ways to continue the trend of scaling by using alternative materials such as Ge and III-V compound semiconductors that could out-perform Si-based CMOS. Although significant progress is made on InGaAs MOSFETs with ALD high-k dielectrics (Al_2O_3, HfO_2, HfAlO, and ZrO_2), GaAs MOSFETs remain a big challenge, mostly showing minuscule drain currents. In this paper, we report on the strong dependence of the electrical properties on different GaAs surface orientations. (111)A Ga polar surface is much more forgiving in terms of Fermi-level pinning for n-channel GaAs MOSFET as shown in Fig.1, compared to (100) Ga-As non-polar surface. It might be directly related with ALD surface chemistry and could be explained by the trap neutral level model. In order to further scale down the equivalent oxide thickness (EOT) of dielectrics, the integration of ALD higher-k ($LaLuO_3$) on GaAs was systematically studied. The precursors lanthanum tris(N,N'-diisopropylformidinate), and lutetium tris(N,N'-diethylformamidinate) reacted with water vapor at 350 °C. The dielectric structures are shown in Fig.2. Fig. 3 shows multi-frequency CV characteristics on n-type and p-type MOS capacitors on GaAs (100) surface with 2 nm Al_2O_3/8 nm $LaLuO_3$/2nm Al_2O_3 as composite dielectric (structure A in Fig. 2). The observed frequency dispersion at accumulation capacitance is comparable to that of pure ALD Al_2O_3. Meanwhile, $LaLuO_3$ with k = 25 to 30 provides a significant advantage in capacitance values. The work verifies the potential to integrate ALD higher-k dielectrics on III-V and deliver 1-2 nm EOT dielectrics by ALD for aggressively scaled ultimate CMOS technology.

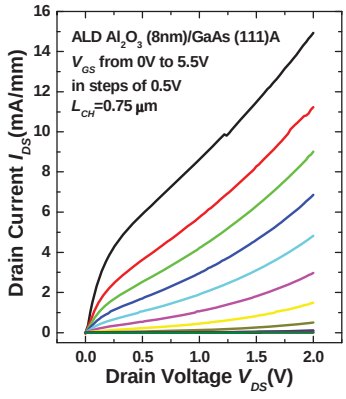


Figure 1 I-V characteristics of an NMOSFET on GaAs (111)A surface with 8nm ALD Al_2O_3 as gate dielectric.

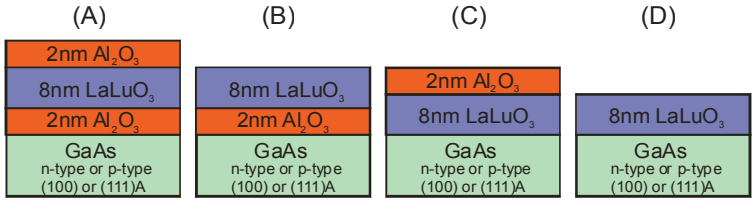


Figure 2 Four $LaLuO_3$ higher-k dielectric structures on GaAs.

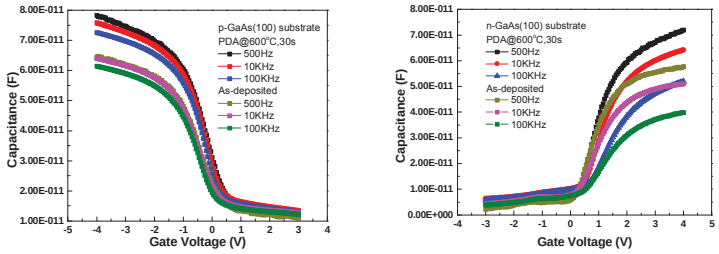


Figure 3 Multi-frequency CV of p-type and n-type GaAs MOS capacitors with the process splits of as-grown and 600°C post -deposition anneal (PDA). The diameter of the capacitors is 100µm.

ALD high-*k* and higher-*k* integration on GaAs

O. Koybasi [1], M. Xu [1], Y. Liu [2], J.-J. Wang [2]
R.G. Gordon [2] and P.D. Ye [1]

1. School of Electrical and Computer Engineering, Purdue University
2. Department of Chemistry and Chemical Biology, Harvard University

Outline

- Motivation
- Brief results on ALD Al_2O_3/GaAs(111)A MOSFET
- ALD Higher-*k* $LaLuO_3$ deposition process
- ALD Higher-*k* $LaLuO_3$ on GaAs (111)A and (100) surfaces

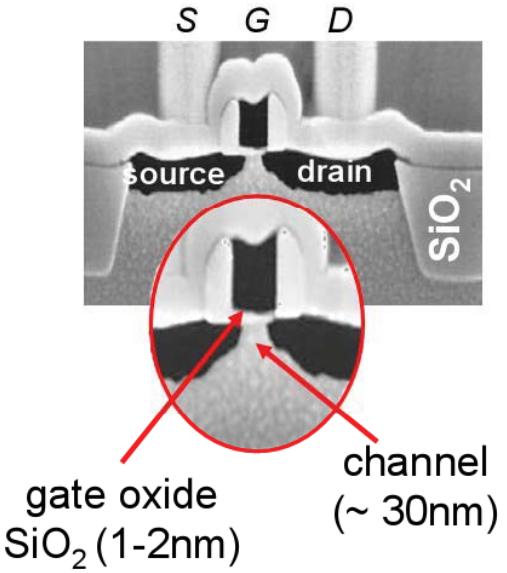
  --- 4 different MIS structures are used to investigate
- Summary

Motivation

1. **Traditional III-V: high frequency and/or high power applications;**
   New III-V thrust: high performance logic applications
   Si based CMOS scaling is going to be end in 2015.
   For 22 nm technology node beyond, it requires novel channel materials such as III-V and high-k

2. **The advantage of III-V as channel materials is high electron mobility.**

3. **Advantage of ALD high-k:**
   --- commercial ALD tools are available
   --- ALD self-cleaning effect on III-V
   --- significant progress on III-V MOSFET in the past 3-5 years using ALD
   --- easy transfer to Si CMOS platform



Si MOSFET (Intel)

	Si	strained Si	bulk Ge	GaAs	GaN	InP	$In_{0.53}Ga_{0.47}As$	InAs	InSb
μ_e	400	1,000	3,900	8,500	1,250	5,400	8,000	20,000	30,000
μ_h	160	240	1,800	400	850	200	300	500	800
E_g (eV)	1.1	1.1	0.66	1.42	3.4	1.35	0.72	0.36	0.18

Inversion GaAs MOSFET: A Historical Dilemma

- Most of inversion GaAs NMOSFETs have minuscule drain current (< 1 mA/mm).
  - F. Ren et al. Solid-State Electronics 41, 1751 (1997)
  - Y. Xuan et al. Appl. Phys. Lett. 88, 263518 (2006)
  - D. Shahrjerdi et al. Appl. Phys. Lett. 92, 203505 (2008)
  - any many others in 70s and 80s.
- **New Solution : our results on GaAs(111)A (next slide)**
- Alternatives:

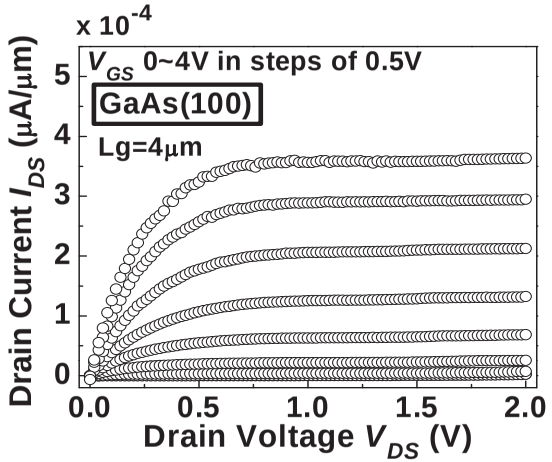
(1) In-rich InGaAs (see recent work by Purdue, Intel, IBM, NTHU, UCSB…)

Potential issue: narrow bandgap material, band-to-band tunneling,…

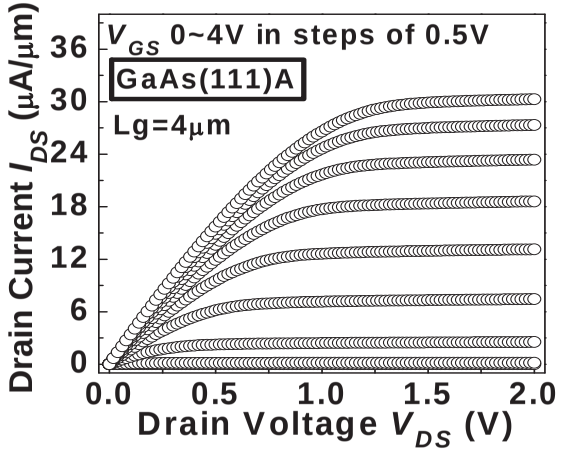
(2) Si interfacial control layer or SiH_4 passivation on GaAs (see recent work by UT Austin, Intel, SUNY Albany, IBM, NUS, UT Dallas,….)

Potential issue: additional SiO_2 increases EOT, inversion mechanism unclear,…

Inversion NMOSFET on GaAs(111)A with Al_2O_3



I_{DS}=3.5x10^{-4} μA/μm

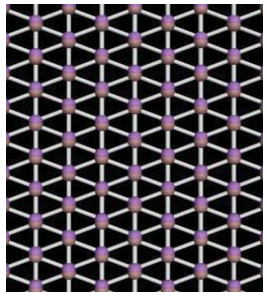


I_{DS}=30 μA/μm

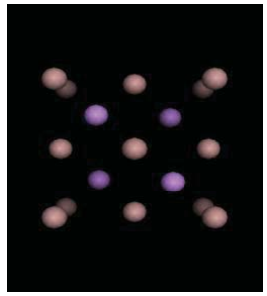
GaAs (100)

X100,000

GaAs (111)A

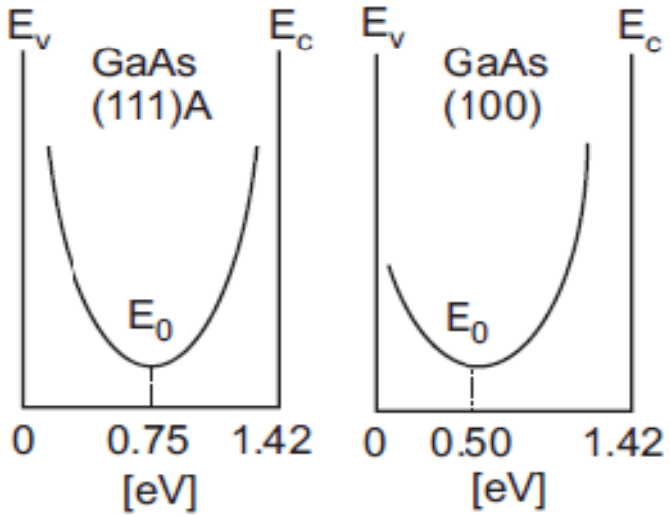


(111)A Ga polar



(100) Ga-As un-polar

Explained by an empirical model
Based on trap neutral level shift



[* M. Xu et al, APL, **94**, 212104, 2009]

[* W.E.Spice et al, JVST, **16**(5), 1979]

Higher-*k* on GaAs for EOT scaling

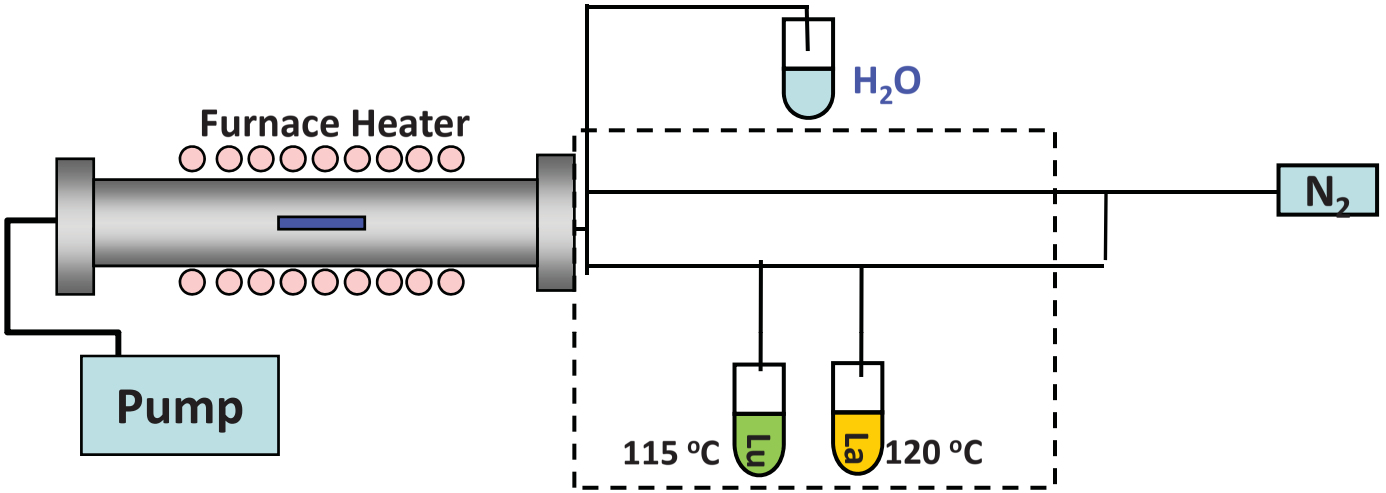
Further application limited due to the small *k* value (8~9) of Al_2O_3

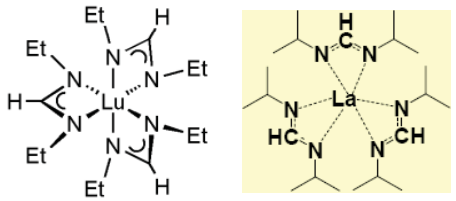
Implementation of higher-*k* gate dielectric $LaLuO_3$ with *k*=24~26 !!!

Questions:

- *How to integrate higher-k $LaLuO_3$ on GaAs or III-V ?*
- *Is it feasible to integrate $LaLuO_3$ directly on GaAs ?*

Higher-*k* dielectric deposition process



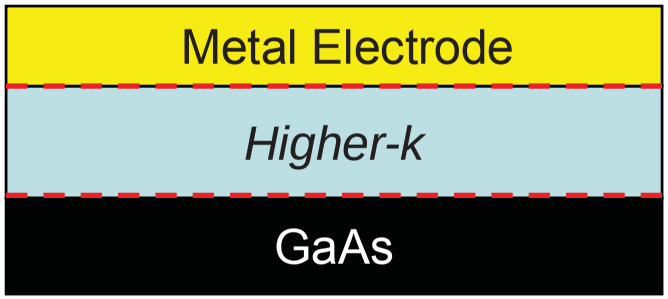


MO precursors	Oxidant	Bubbler temp.	Deposition temp.	La_2O_3 : Lu_2O_3
$La(amd)_3$ $Lu(amd)_3$	DI H_2O	120°C for La 115°C for Lu	350 °C	1:1

[* provided by Y. Liu in Prof. Roy Gordon's group at Harvard]

Requirements for higher-*k* integration

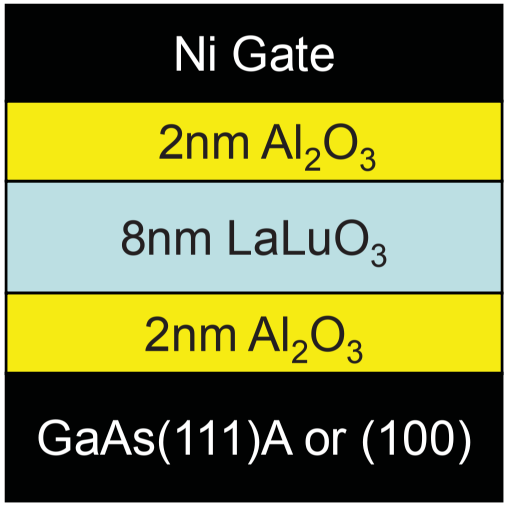
(4)



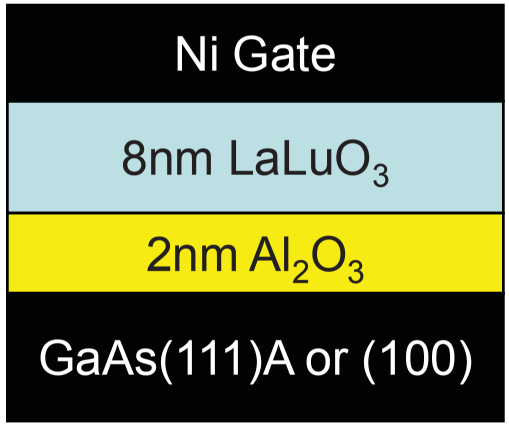
Compatible?

- Different MIS structures to be studied

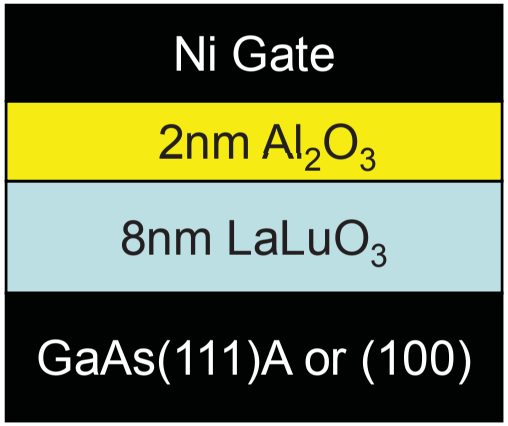
  each structure splits into two:
  - as-deposited
  - PDA@600°C,30s in N_2



(1)

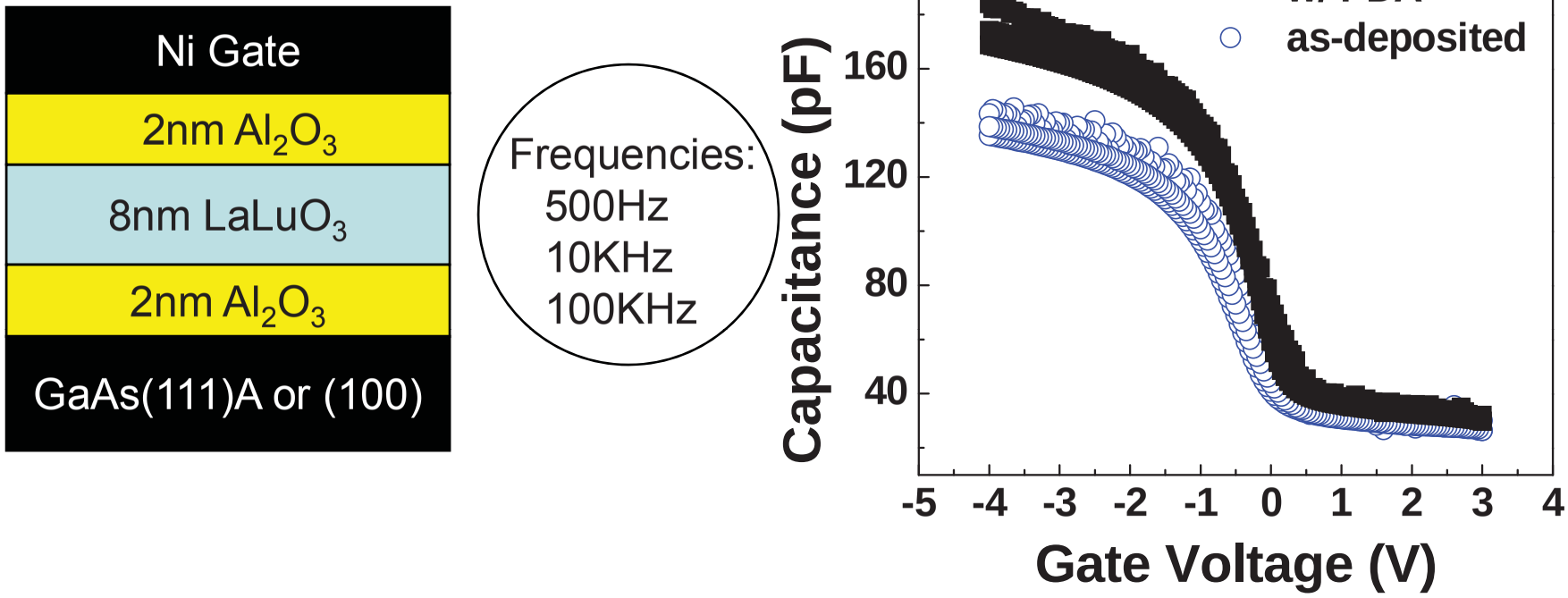


(2)



(3)

C-V characteristics on p-type GaAs

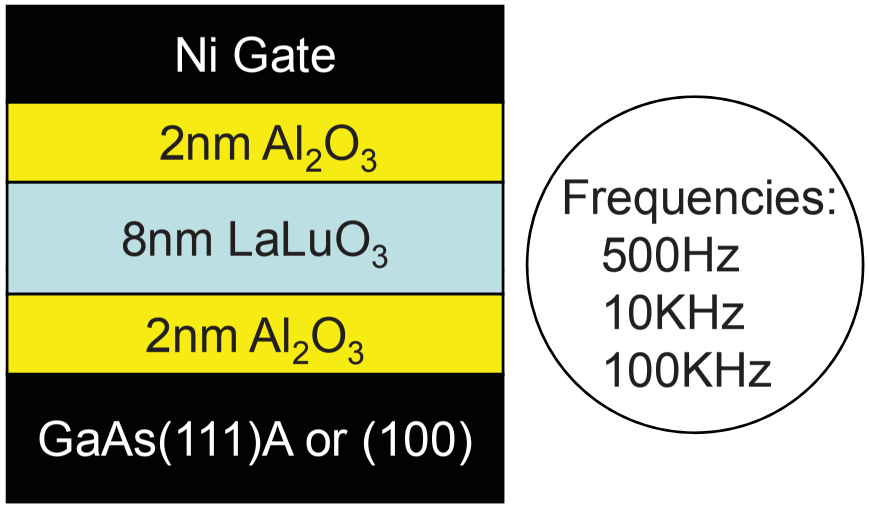


■ Capacitance increased after annealing due to water-adsorptive property of La-based dielectric

■ All p-type GaAs MOS CVs are "good-looking" with less frequency-dispersion at accumulation, which includes (100), (111)A with Al_2O_3, HfO_2, HfAlO and LLO.

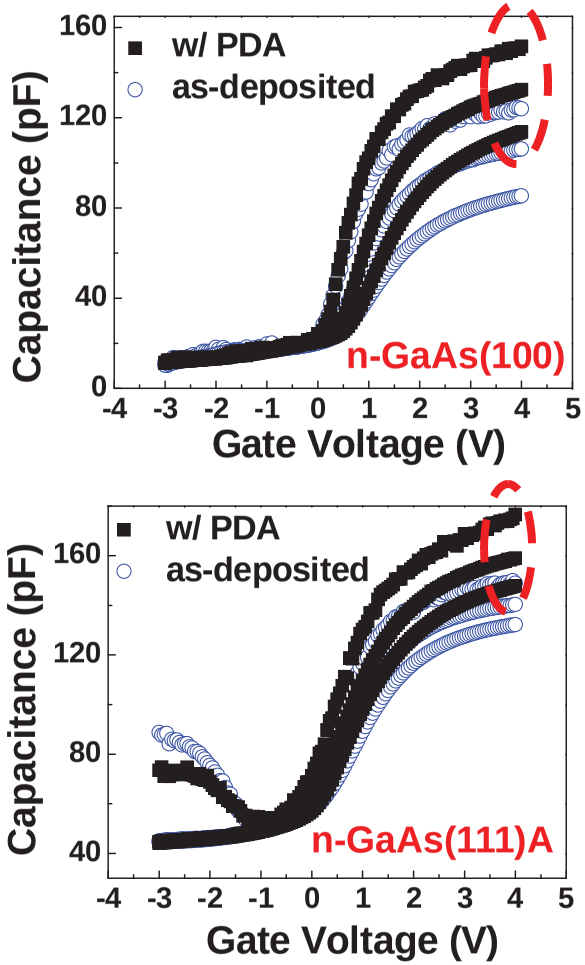
■ It relates with ALD "self-cleaning effect" on As_2O_3, As_2O_5,… (see Frank et al. 2005, Huang et al. 2005, Hinkle et al. 2007, and others) and lower half band-gap of GaAs has less problem.

C-V characteristics on Structure (1)



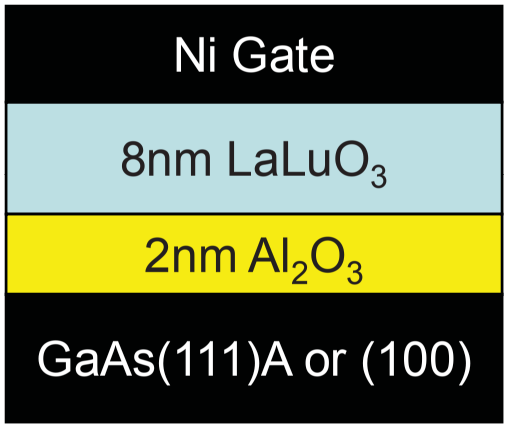
Frequencies:
500Hz
10KHz
100KHz

EOT: ~3.3nm

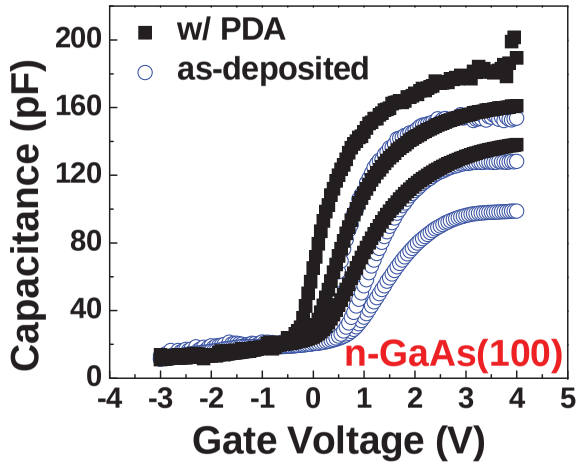


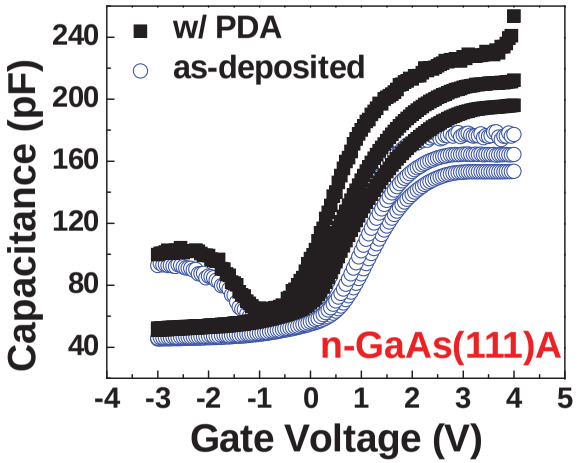
- Frequency dispersion on (111)A is better than that on (100)
- Lower D_{it} along upper half band-gap of GaAs(111)A
- EOT~3.3nm, *k* value is extracted to be ~24

C-V characteristics on Structure (2)



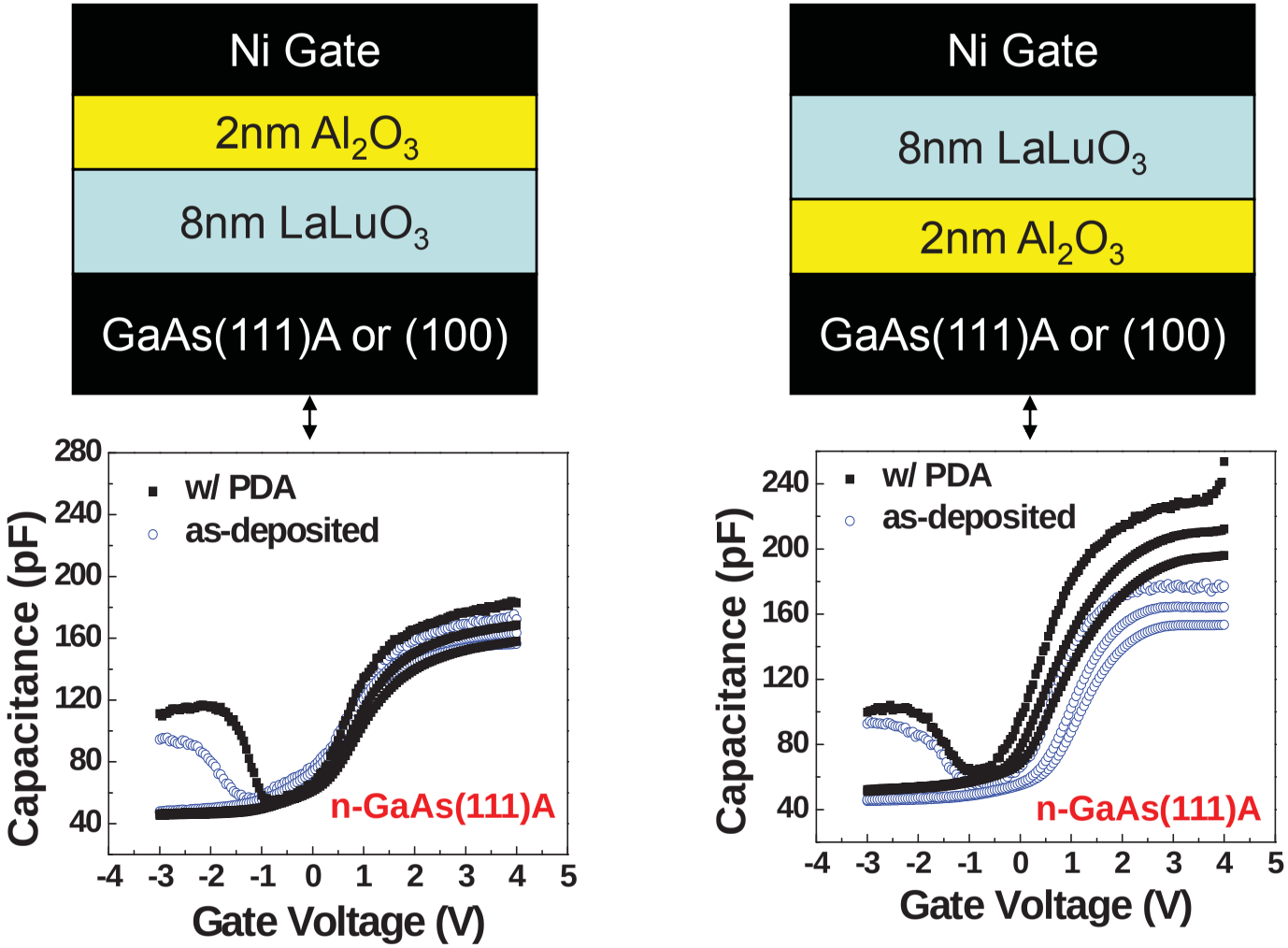
EOT: ~2.3nm





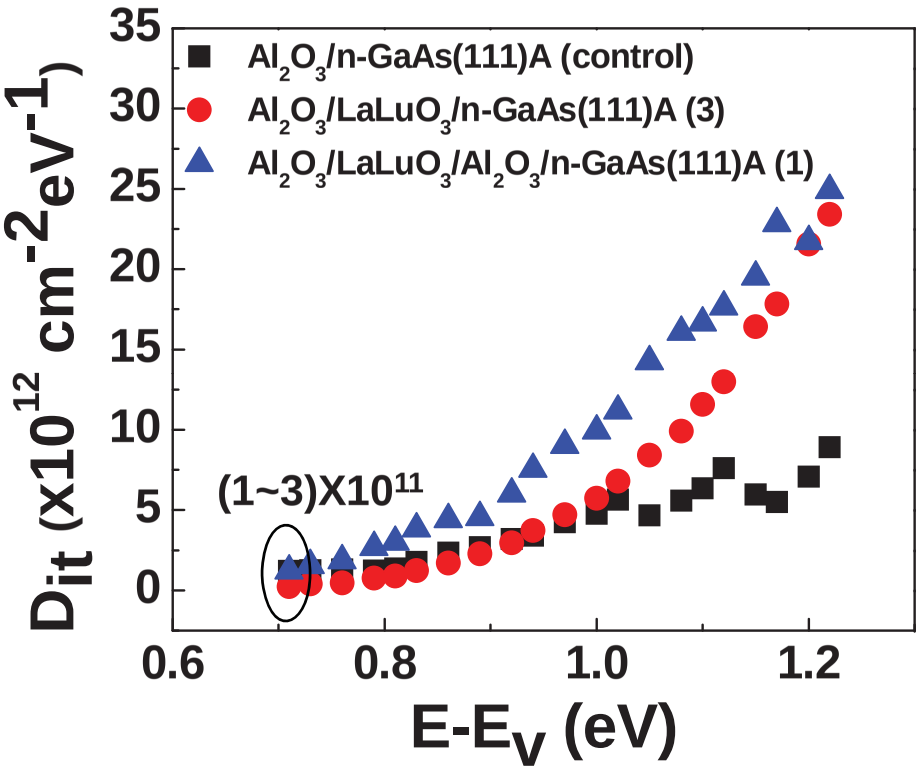
- Capacitance increased as expected and EOT scaled down to 2.3nm
- Exactly due to the removal of Al_2O_3 capping layer of 1nm EOT
- No additional interface layer introduced by metal/higher-*k* direct contact

C-V characteristics on Structure (3)



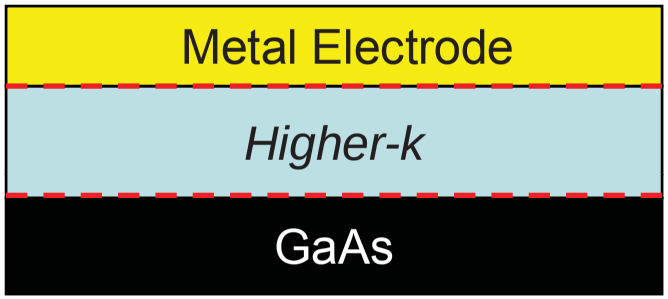
- Surprisingly, capacitance didn't obviously increased after annealing
- Some interfacial layer may be introduced at higher-*k*/GaAs interface
- Will this extra-layer influence the interface quality?

Interface Trap Density on GaAs(111)A



- D_{it} was extracted by *HF-LF* method
- (3) almost has the same D_{it} as the control sample, but has higher D_{it} to the E_C edge
- Surprisingly even with Al_2O_3 ICL, (1) has higher D_{it} than (3)

Pure higher-*k* direct on GaAs



No reasonable C-V characteristic obtained !!!

Possible Problems:

Two interfaces shows good quality respectively, Why doesn't it work with pure higher-*k* direct on GaAs? Small conduction band offset ??

Further investigation needed !!!

Summary

- Inversion NMOSFET is realized by integration of ALD Al_2O_3 on GaAs(111)A
- Higher-*k* $LaLuO_3$ is first demonstrated to be integrated on GaAs

  --- metal/$LaLuO_3$ interface quite stable

  --- Al_2O_3/$LaLuO_3$/GaAs has comparable interface as Al_2O_3/GaAs

  --- Al_2O_3/$LaLuO_3$/GaAs interface may introduce additional layer after PDA
- Further study on metal/$LaLuO_3$/GaAs is needed

We acknowledge the valuable discussions and on-going collaboration with Prof. R.M. Wallace's group at UT Dallas. The work is partly supported by NSF, SRC FCRP MSD Center, and DoD ARO.