Atomic layer deposition of gadolinium scandate films with high dielectric constant and low leakage current

Kyoung H. Kim and Damon B. Farmer
Division of Engineering and Applied Sciences, Harvard University, Cambridge, Massachusetts 02138

Jean-Sebastien M. Lehn, P. Venkateswara Rao, and Roy G. Gordon[a)]
Department of Chemistry and Chemical Biology, Harvard University, Cambridge, Massachusetts 02138

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$GdScO_3$ films were deposited on hydrogenated silicon substrates by atomic layer deposition. The films were pure and amorphous, both as-deposited and after a 5 min anneal at 950 °C. Cross-sectional transmission electron microscopy revealed a sharp, smooth interface between $GdScO_3$ and Si. Capacitance and leakage current measurements on metal oxide semiconductor capacitors made from atomic layer deposited $WN/GdScO_3$ stacks showed that the amorphous $GdScO_3$ films have a high dielectric constant (~22), low fixed charge density, and low interface trap density. A film with 1 nm equivalent oxide thickness also demonstrated that the leakage current density is less than 2 mA/cm^2 at 1 V gate bias. © *2006 American Institute of Physics*. [DOI: 10.1063/1.2354423]

Since the introduction of metal oxide semiconductor (MOS) field-effect transistors (FETs) as the centerpiece of microelectronic devices, the miniaturization of transistor size has continued in order to improve transistor performance. Correspondingly, the thickness of SiO_2-based gate dielectrics has been scaled down to keep the transistor drive current high enough to sustain speed enhancement. The thickness requirement for gate dielectric layers specified in the current and future roadmap has become so small that the leakage current density will be prohibitively high if SiO_2-based films are used as gate dielectrics.[1] One solution to this problem is the integration of high-κ dielectrics into gate stacks. Recent developments in employing high-κ dielectric layers have centered on hafnium based dielectrics. The main limitation of Hf-based dielectrics is that they require either a significantly thick (>0.5 nm) SiO_2 interlayer or must be alloyed with SiO_2 to form silicates that have lower dielectric constants, thereby limiting the future scalability.[2]

In this respect ternary rare earth oxides such as lanthanum aluminate have drawn interest as possible candidates for the next generation of high-κ materials. Among these oxides, rare earth scandates such as lanthanum scandate ($LaScO_3$), dysprosium scandate ($DyScO_3$), and gadolinium scandate ($GdScO_3$) have been studied actively because of their promising properties. Recent reports on thin films of $GdScO_3$ deposited by pulsed layer deposition[3] and e-beam evaporation[4] demonstrate that amorphous $GdScO_3$ films possess a dielectric constant comparable to HfO_2 ($\kappa \sim 22-23$) and low leakage current. It was also shown that the films stay amorphous after annealings under conditions similar to those of the conventional source/drain dopant activation process for Si MOSFETs. These reports illustrate many of the desirable properties of $GdScO_3$ as a gate dielectric, and motivate the development of an atomic layer deposition (ALD) process for this material. ALD offers excellent film uniformity over a large area and provides high conformality that is required for aggressive device geometries, and the processes can be easily adopted for large-scale production. Furthermore, control of the SiO_x interlayer thickness below 0.5 nm has yet to be demonstrated clearly, which leaves a question as to the ultimate scalability of $GdScO_3$ films. In this study, we show that $GdScO_3$ films can be deposited by ALD with minimal interlayer thickness (~0.15 nm) while maintaining their desirable electrical and structural properties.

We have previously reported ALD of scandium oxide[5] and other lanthanide oxides[6] from metal amidinate precursors. The precursors used in this study are also metal amidinate precursors: scandium tris(N,N'-diethylacetamidinate) or $Sc(Et_2\text{-Me-amd})_3$ for scandium oxide, and gadolinium tris(N,N'-diisopropylacetamidinate) or $Gd(iPr_2\text{-Me-amd})_3$ for gadolinium oxide. These precursors have chelating nitrogen to metal bonds, which provide inherent thermal stability. We did not find evidence of thermal decomposition of these precursors at temperatures up to 320 °C in the time scale of our ALD process. Also, both of the precursors possess high reactivity with H_2O, and the reactions result in metal oxide films and volatile amidine byproducts.

Synthesis of the $Gd(iPr_2\text{-Me-amd})_3$ precursor was done using the protocol outlined in Lim *et al.*[7] It was made in high yield (>80%) and thermogravimetric analysis (TGA) revealed residue of only 1.4% after a 10 °C/min ramp to 500 °C, indicating that $Gd(iPr_2\text{-Me-amd})_3$ has high thermal stability. The precursor starts to sublimate at 125 °C and 20 mTorr. Synthesis of $Sc(Et_2\text{-Me-amd})_3$ requires a slightly different route. First, the amidine H[EtNC(Me)NEt] was prepared by a modification of the procedure recently reported,[8] and *n*-BuLi was added to a solution of the amidine in diethylether to make lithium N,N'-diethylacetamidinate or $Li(Et_2\text{-Me-amd})$. The reaction between $Li(Et_2\text{-Me-amd})$ and $ScCl_3$ yields the $Sc(Et_2\text{-Me-amd})_3$ compound after a filtration and purification process. The sublimation was carried out at 90 °C and 20 mTorr, and the final yield was 57.2%. TGA showed that the residue was only 0.6% after a 10 °C/min ramp to 500 °C.

$GdScO_3$ films were deposited in a horizontal gas flow reactor[9] using H_2O vapor and aforementioned metal amidinate precursors $Sc(Et_2\text{-Me-amd})_3$ and $Gd(iPr_2\text{-Me-amd})_3$. The bubblers holding the metal amidinates were kept at

a)Electronic mail: gordon@chemistry.harvard.edu

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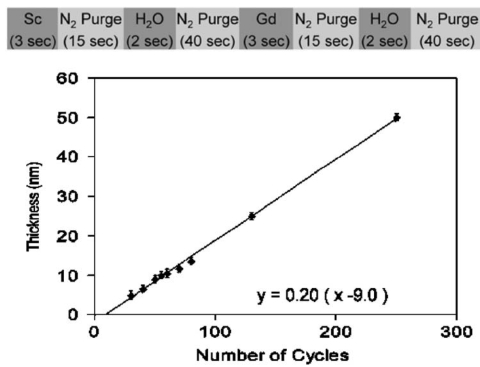

FIG. 1. (a) Pulse sequence of $GdScO_3$ ALD. (b) Thickness as a function of cycle number. Thickness determined by ellipsometry. Films were deposited on HF last silicon at 310 °C.

140 °C, and the substrate temperature for the deposition was 310 °C. The substrates used were *n*-type and *p*-type Si (100). Before deposition, the substrates were treated with UV/ozone to remove organic contaminants, and then dipped in 5% aqueous HF solution for 1 s to achieve a hydrogen-terminated surface. Film thickness and uniformity were measured using a single wavelength (632.4 nm) scanning ellipsometer (Gaertner Scientific, LSE-W). Separate depositions of Gd_2O_3 and Sc_2O_3 yielded the same growth rate of 1.0 Å/cycle. One cycle of $GdScO_3$ ALD was set as the sequential dosing of $Sc(Et_2\text{-Me-amd})_3$, H_2O, $Gd(iPr_2\text{-Me-amd})_3$, and H_2O with a purging sequence following each dose [Fig. 1(a)]. The resulting film thickness was linearly proportional to the number of cycles [Fig. 1(b)], which is one of the defining characteristics of a self-limiting ALD process. The growth rate was measured to be 2.0 Å/cycle with slight inhibition during the first several cycles. The film thickness was uniform (less than 5% variation) over a distance of at least 20 cm. The refractive index of the films determined by spectroscopic ellipsometry ranged from 1.95 to 1.99.

To obtain film composition and impurity content, Rutherford backscattering spectroscopy was performed. Some of the films were deposited on amorphous carbon substrates to increase sensitivity to light elements. The stoichiometry was found to be $Gd_{1.0}Sc_{1.1}O_{3.2}$, which means that the films are slightly scandium rich. Carbon and nitrogen concentrations were below the detection limit (<1 at. %). Glancing angle x-ray diffractometry analysis indicated that the films were amorphous as deposited. Furthermore, the films stayed amorphous after a 5 min anneal at 950 °C in forming gas, which agrees with the results of a previous report on $GdScO_3$.[4] Using atomic force microscopy, the root mean square roughness of the as-deposited films was determined to be approximately 2 Å, and the roughness did not change after high-temperature annealings.

ALD tungsten nitride (WN) was used as a gate metal, which offers several advantages. It is an excellent diffusion barrier for metal and oxygen atoms, and has good adhesion to most metals and oxides.[10] WN is also thermally stable, decomposing to W only after long anneals at temperatures above 850 °C. Also, the etch rate of WN by reactive ion etching (RIE) using a fluorine-based chemistry is fairly high and the by-product (WF_6) is volatile at room temperature. Bis(tert-butylimido)bis(dimethylamido) tungsten (VI) and ammonia gas were used as precursors for WN ALD.[10] The deposition temperature for WN ALD was 385 °C, at which temperature the growth rate is 2.5 Å/cycle. The resistivity of WN was approximately 4000 $\mu\Omega$ cm, and the carbon concentration in the film was less than 8 at. %.

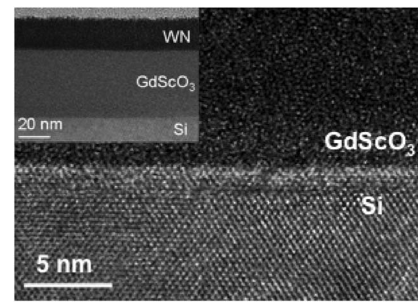

FIG. 2. High resolution TEM micrograph of a WN/$GdScO_3$ stack on Si. Both WN/$GdScO_3$ and $GdScO_3$/Si interfaces are sharp and smooth.

Figure 2 shows high resolution cross-sectional transmission electron microscopy (TEM) micrographs of a WN/$GdScO_3$ stack on (100) Si. The thicknesses of $GdScO_3$ and WN were 40 and 20 nm, respectively. The stack was annealed at 500 °C for 5 min in forming gas prior to imaging. The images demonstrate that both $GdScO_3$ and WN films are uniform in thickness and homogeneous in density. The absence of lattice fringes in the $GdScO_3$ film is in contrast to the distinct lattice of the Si, confirming that the $GdScO_3$ film is amorphous. The WN/$GdScO_3$ and $GdScO_3$/Si interfaces are smooth and abrupt. Most importantly, the transition from Si to $GdScO_3$ is lacking any amorphous low-κ SiO_x interlayer.

For electrical analysis, multiple MOS capacitors were made out of WN/$GdScO_3$ stacks on Si. The thicknesses of the WN layers were fixed to 20 nm, while the $GdScO_3$ layers varied in thickness from 4 to 20 nm. Pt was deposited through a shadow mask to serve as an etch mask and top contact. WN was then etched by CF_4 RIE through the etch mask to form capacitor structures. All of the capacitors then underwent rapid thermal anneal at 500 °C for 5 min in forming gas. High frequency (100 kHz, 1 MHz) capacitance-

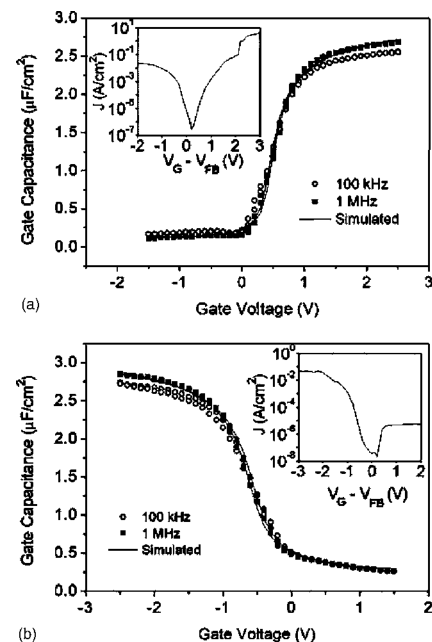

FIG. 3. *C-V* curves at 1 MHz and 100 KHz for a stack with a 4.9 nm $GdScO_3$ layer. EOTs are (a) 1.0 nm on the *n*-type substrate and (b) 0.95 nm on the *p*-type substrate. Insets show leakage current density vs gate voltage bias.

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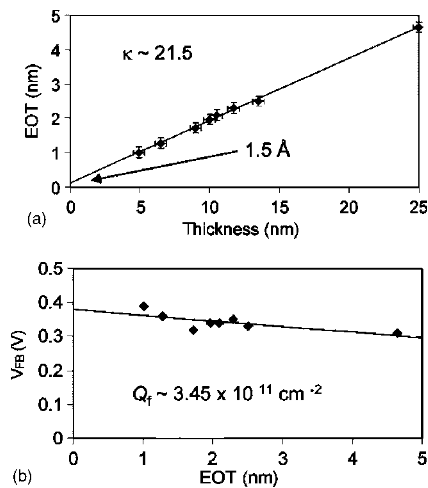

FIG. 4. (a) EOT plotted as a function of film thickness. The dielectric constant from the slope of the linear fit is 21.5, and the intercept is 1.5 Å. (b) Flatband voltage as a function of EOT. The fixed charge density is 3.45 $\times 10^{11}$ cm^{-2}, and the work function of WN is 4.6 eV.

voltage (*C*-*V*) and dc leakage current-voltage measurements were then carried out on the resulting capacitors.

C-*V* curves for two MOS capacitors made of WN/$GdScO_3$ stacks on *n*-type and *p*-type Si substrates are shown in Fig. 3. The thickness of the $GdScO_3$ layer is 4.9 nm for both capacitors. The *C*-*V* curves have ideal shapes without any noticeable humps or stretching, which implies good interface quality. The hystereses of the curves were 20 mV for *n* type and 50 mV for *p* type. These low hysteresis values indicate that the dielectric does not have many bulk charge traps. The curves at 100 kHz and 1 MHz are closely aligned, indicating little frequency dispersion, which suggests that the film is relatively free of hydroxyl groups.[11] To obtain the equivalent oxide thickness (EOT) and the flatband voltage values, the *C*-*V* data were fit to ideal curves using the Hauser and Ahmed simulation program.[12] The experimental curves show excellent agreement with the simulated curves. The EOT values with quantum corrections were 1.01 nm for the device on the *n*-type substrate and 0.95 nm on the *p*-type substrate. The flatband voltages were +0.39 V for *n* type and −0.59 V for *p* type. From the corresponding gate leakage density curves (insets of Fig. 3), the leakage current density $<2\times 10^{-3}$ A/cm^2 at 1 V gate voltage bias ($|V_G\text{-}V_{FB}|$).

The dielectric constant of the films and the interfacial layer (IL) thickness are obtained from the EOT versus thickness plot shown in Fig. 4(a). The slope of the linear fit can be used to extract the dielectric constant, and the *y* intercept provides a good estimate of the IL thickness. This method gives a dielectric constant of 21.5 for our ALD $GdScO_3$ films, which is close to the values reported previously.[3,4] The estimated IL thickness is approximately 1.5 Å, which indicates very good scalability of our ALD $GdScO_3$ films. Figure 4(b) shows a plot of the flatband voltages with respect to the corresponding EOTs. The fixed charge density calculated from the slope of the linear fit is 3.45×10^{11} cm^{-2}.[13] The work function of WN obtained from the *y* intercept is 4.6 eV, which means that WN is a midgap metal. The interface trap density was obtained from high frequency conductance measurements on the MOS capacitors and was found to be 3.0×10^{11} cm^{-2} eV^{-1}.[13] The reasonably low values of the fixed charge density and the interface trap density mean

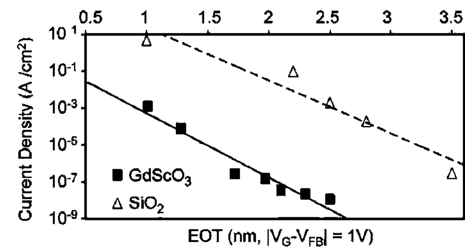

FIG. 5. Leakage current density at 1 V of $|V_G\text{-}V_{FB}|$ with respect to EOT for $GdScO_3$ and SiO_2. The leakage current density of $GdScO_3$ is about four orders of magnitude smaller than that of SiO_2.

that the MOSFET devices made from these gate stacks should have relatively high carrier mobility.

Another important aspect to consider when discussing scalability of a dielectric is how its leakage current density increases with respect to decreasing EOT. Figure 5 shows the leakage current density scaling of our ALD $GdScO_3$ films compared to that of thermal SiO_2 films. The leakage current density of our ALD $GdScO_3$ films is about four orders of magnitude lower than that of thermal SiO_2 films and is in a range similar to those of other high-κ films such as HfO_2 and $LaAlO_3$.

In summary, $GdScO_3$ films were deposited by ALD using thermally stable scandium amidinate and gadolinium amidinate precursors, and H_2O. The films were amorphous as deposited and stayed amorphous after high temperature annealing. Electrical measurements on gate stacks of ALD WN/$GdScO_3$ showed that $GdScO_3$ has a dielectric constant of 21.5 and an interlayer thickness of approximately 1.5 Å. Leakage current densities of $<2\times 10^{-3}$ A/cm^2 at 1 V gate voltage bias for films with EOTs as low as 1 nm were demonstrated. Furthermore, the fact that the ALD $GdScO_3$ films have low fixed charge density and low interface trap density means that $GdScO_3$ is a promising candidate for a next generation gate dielectric.

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