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Direct-Liquid-Evaporation Chemical Vapor Deposition of Nanocrystalline Cobalt Metal for Nanoscale Copper Interconnect Encapsulation

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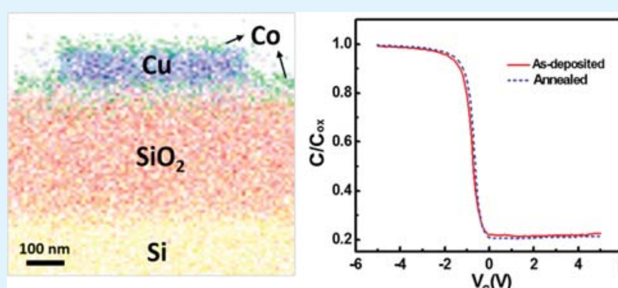
S *Supporting Information*

ABSTRACT: In advanced microelectronics, precise design of liner and capping layers become critical, especially when it comes to the fabrication of Cu interconnects with dimensions lower than its mean free path. Herein, we demonstrate that direct-liquid-evaporation chemical vapor deposition (DLE-CVD) of Co is a promising method to make liner and capping layers for nanoscale Cu interconnects. DLE-CVD makes pure, smooth, nanocrystalline, and highly conformal Co films with highly controllable growth characteristics. This process allows full Co encapsulation of nanoscale Cu interconnects, thus stabilizing Cu against diffusion and electromigration. Electrical measurements and high-resolution elemental imaging studies show that the DLE-CVD Co encapsulation layer can improve the reliability and thermal stability of Cu interconnects. Also, with the high conductivity of Co, the DLE-CVD Co encapsulation layer have the potential to further decrease the power consumption of nanoscale Cu interconnects, paving the way for Cu interconnects with higher efficiency in future high-end microelectronics.



KEYWORDS: *cobalt, copper encapsulation, metal interconnect, DLE-CVD, nanocrystalline*

1. INTRODUCTION

Continued progress in the downsizing of microelectronic devices has brought great challenges in many fields, especially interfacial engineering and interconnect fabrication at nanometer scales.[1,2] As a critical part of transmitting signals among microelectronic units, metal interconnect architectures have been calling for exponentially increased integration density and complexity in the past decades.[3] One of the greatest obstacles limiting the industry from further scaling down copper (Cu) interconnects, which is the most widely used interconnect material, is the electromigration (EM) and diffusion of Cu.[4−6] Various barrier, liner, and capping layers for Cu interconnects have been reported in the effort to stabilize Cu atoms by suppressing their diffusion and migration, including SiN_x, SiCN, and transition-metal nitrides.[7−9] However, when it comes to a 22 nm technology node and below, dimensions of interconnects are already less than the mean free path (MFP) of Cu (∼40 nm), while Cu metal conductivity decreases exponentially as it shrinks in size below MFP due to surface and grain boundry scattering.[10−12] As a result, by adding several nanometers of a low-conductivity tantalum nitride barrier layer (∼10^6 S/m) onto Cu (5.96×10^7 S/m), the effective width of a Cu wire would be decreased by 10−20%, thus drastically decreasing the overall conductivity of the nanoscale interconnects.[13,14] Therefore, a high-conductivity metallic material with Cu stabilization functionalities is needed for further-down-sized microelectronic interconnects.

Cobalt (Co) and Co alloys are known as effective capping layers that are capable of suppressing surface electromigration of Cu at macroscopic scales.[15,16] Furthermore, since Co has a high bulk metallic conductivity of 1.60×10^7 S/m and an estimated MFP of only ∼16 nm at room temperature, it is emerging as a promising candidate for advanced Cu liner/capping layers.[17,18] Traditionally, Co metal was deposited by PVD methods that do not have the capability of coating inside high-aspect-ratio structures.[19] Thus, metal−organic chemical vapor deposition (MOCVD) with cobalt carbonyl precursors [e.g., $Co_2(CO)_8$] was introduced for better conformality.[20] However, cobalt carbonyl precursors have poor thermal stability and narrow practical deposition temperature windows, and usually lead to a rough film with surface roughness rms greater than 2.2 nm.[21] Recently, our group reported novel direct-liquid-evaporation chemical vapor deposition (DLE-CVD) methods for metal and metal nitride thin films, which provided the feasibility to create higher-quality Co films over a wide range of deposition temperatures and low chance of predeposition decomposition of precursors.[22,23]

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When a precursor is vaporized from a conventional bubbler, the actual rate of vapor delivery is subject to many variables, including drifts in the bubbler temperature, the amount of precursor remaining in the bubbler, and thermal decomposition during long times at high temperatures. In contrast, precursors in DLE-CVD systems are stored at room temperature, such that thermally induced decomposition is negligible. The residence time of the precursor vapor in the heated evaporation region is also very short, minimizing the decomposition of the precursor during the vaporization. The precursor delivery rate is stably controlled and measured by a liquid flow controller immediately before it flows into the evaporation region.[24] In making nanoscale metal interconnects, it is critical to have precise control over all deposition processes to guarantee reliability and reproducibility. For liners and capping layers of copper interconnects, it is particularly important to design deposition conditions that create continuous and pinhole-free films with nanosized crystallinity for blocking the diffusion of copper.[25]

In this report, we use nanoscale elemental imaging and electrical measurements to demonstrate that precisely controlled DLE-CVD of Co metal films is a promising liner and capping layer for nanoscale Cu interconnects. Narrow Cu wires encapsulated all-around by DLE-CVD Co were fabricated as illustrated in Figure 1. In-depth study of temperature-dependent deposition characteristics and atom probe tomography (APT) analysis are conducted to understand better the kinetics of DLE-CVD Co growth and its atomic-scale morphology. APT imaging studies showed that our DLE-CVD Co forms a smooth nanocrystalline film with a grain size of ∼10 nm and surface roughness rms of ∼0.9 nm. Electrical measurements on microcapacitors show that Cu is effectively blocked from diffusing into the SiO_2 dielectric layer by our DLE-CVD Co. This work provides direct evidence that encapsulating nanoscale Cu interconnects with nanocrystalline DLE-CVD Co can substantially improve its stability and suppress diffusion of Cu atoms, paving the way for improved Cu interconnects in advanced microelectronics.

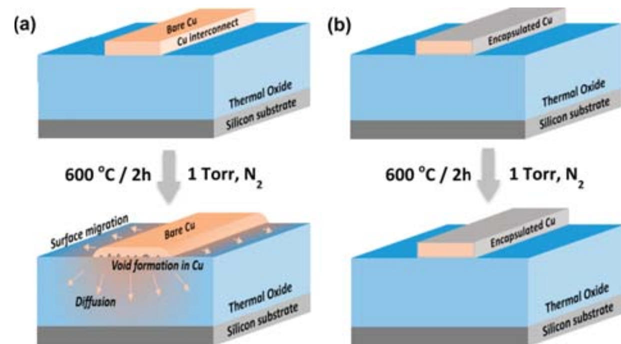

Figure 1. Schematic illustration of preventing the diffusion and deterioration of nanoscale Cu interconnects by DLE-CVD Co encapsulation. (a) Bare Cu interconnect; (b) Cu interconnect with DLE-CVD Co encapsulation.

2. EXPERIMENTAL SECTION

Co DLE-CVD Details. The precursor used in this work is a cobalt amidinate, bis(*N,N*′-diisopropylacetamidinato) cobalt(II) (Figure S1, Supporting Information), which has been reported previously.[23,26] Tetradecane (Millipore Sigma Chemical Co.) was distilled from sodium to remove moisture before use. All chemical operations were conducted in a glove box with a nitrogen atmosphere. Cobalt precursor solution was prepared by dissolving 5 g of Co precursor in 50 mL of tetradecane. The CVD of Co is conducted with a homemade direct-liquid-evaporation (DLE) system (Figure S2). During the deposition process, a precisely controlled precursor solution flow (12 wt % in tetradecane) is injected into and vaporized in a heated vaporization loop, in which a constant 100 cubic centimeters per minute (sccm) of N_2 is flowing as a carrier gas. Then the precursor vapor is mixed with 100 sccm purified ammonia (NH_3) and 100 sccm hydrogen (H_2) as co-reactant gases, and delivered into a preheated deposition chamber (16 in. long and 1.25 in. diameter) with an 11 in. × 1.25 in. semicylindrical sample holder inside. The total pressure in the reactor chamber is also regulated and maintained at 10 Torr in which the partial pressures of NH_3, H_2, and N_2 all equal 3.23 Torr. The Co precursor partial pressure varied from 0.02 to 0.08 Torr in this work. On the basis of the calculation of reaction zone volume and flow rates, it takes roughly 13 s for a precursor molecule to be delivered across the reaction zone on statistical average.

APT Sample Preparation and Analysis Parameters. The Cameca LEAP 4000X HR system was used for APT analysis. Twenty-five nanometers of Co films by different deposition conditions were deposited onto presharpened silicon microtips (PSMs). The final needle-shaped specimens have a tip radius between 50 and 70 nm, and with shank angles around 10°. The analyses were carried out at 40 K under a vacuum pressure lower than 5×10^{-11} Torr. A 532 nm laser with 50 pJ pulse energy was used to assist ion evaporation at a pulse frequency of 100 kHz. Data reconstruction was performed with IVAS software (Cameca, Gennevilliers, France), extracting three-dimensional quantitative compositional and structural information.[27]

Fabrication of Trench Test Structure. A flat silicon chip was first coated with 2 μm of positive photoresist as a soft mask, and patterned with 500 μm wide, 0.5 cm long exposed lines by photolithography. A 500 μm wide, 2 μm deep shallow trench was created by a Bosch-type deep silicon reactive ion etching (DRIE) process with SF_6 and C_4F_6 gases, and thoroughly cleaned afterward. Finally, the chip was physically capped with another flat silicon chip to cover part of the 0.5 cm length, leaving one end exposed as the opening of the parallel deep trench.

Microcapacitor Fabrications and Measurements. To evaluate the copper barrier performance of DLE-CVD Co, a p-type silicon chip with 50 nm thermal oxide layers was coated with 10 nm DLE-CVD Co at 200 °C followed by 50 nm PVD Cu, and then annealed at 600 °C for 1 h under 1 Torr of flowing N_2. After annealing, the Cu and Co films were removed by wet etching to fabricate microcapacitors. Square-shaped Au electrodes (50 μm × 50 μm) were then fabricated by standard photolithography, metallization, and lift-off process. For comparison, nonannealed samples were also fabricated into microcapacitors. The microcapacitors were measured by a probe station with a Keysight E4980A precision LCR meter. Capacitance versus voltage (*C*−*V*) characteristics were measured at 2 MHz with a sweep rate of 0.2 V/s. All measurements started at positive 5 V and scanned from positive bias toward negative bias.

Other Characterization Details. The cross-sectional morphology of the films was visualized with a Zeiss Ultra Plus field-emission scanning electron microscope (FE-SEM), from which the thickness of each film was measured. A Zeiss Ultra55 with EDAX detector was used to acquire EDAX mapping images. The depth-profile elemental analysis was carried out by Thermo Scientific K-Alfa X-ray photoelectron spectroscopy (XPS). A JEOL 2100 transmission electron microscope was used to study microscopic crystallography for which the samples were prepared onto a TEM grid with an ultrathin silicon nitride membrane. X-ray diffraction patterns were acquired by a Bruker D2 Phaser. Surface morphology of the films was analyzed by atomic force microscopy (AFM) (Asylum Model MFP-3D AFM system). Step coverage evaluation of DLE-CVD Co was conducted on a planar trench structure as shown in Figure S3 and Figure S4. The nanoscale Cu lines for Cu encapsulation were patterned by an Elionix F-125 ultra-high-precision electron beam lithography system, and metallized by electron beam evaporation of Cu.

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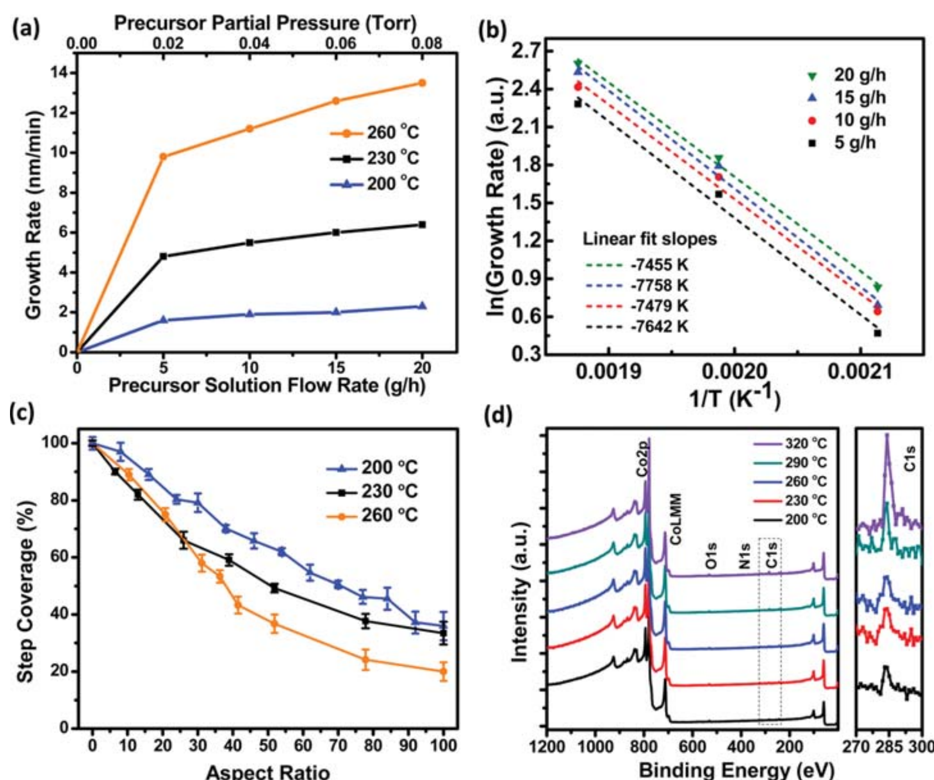

Figure 2. (a) Precursor flow-dependent growth rate plot at different deposition temperatures; total pressure is 10 Torr in all experiments. (b) Arrhenius plots and linear fits at different precursor flow rates. (c) Step coverage along a horizontal trench test structure (measurement method illustrated in Figure S4 in the Supporting Information). (d) XPS survey scans of DLE-CVD Co samples deposited at different temperatures; the boxed region is the C 1s peak, which is magnified in the graph on the right side.

3. RESULTS AND DISCUSSION

To understand the deposition process of DLE-CVD cobalt metal, we conducted a series of temperature-dependent studies. In all depositions, co-reactant gas flows are set to be 100 sccm NH_3 and 100 sccm H_2, and the precursor solution concentration is fixed at 12 wt %, which were evaluated to be the best conditions for high conformality and smoothness according to our previous report.[23] Figure 2a plots the growth rates of DLE-CVD Co versus precursor solution flow rates at different temperatures. The results show that our deposition process is highly controllable by precisely setting precursor flow rates and temperatures. A lower temperature with a lower flow rate is suitable for nanoscale applications such as local interconnect and nanoscale capping layer, while a higher temperature with higher flow rate is favorable for larger-scale coatings such as intermediate and global interconnects in 3D microelectronics.[7] By plotting the natural logarithm of growth rate versus the reciprocal of temperature (Figure 2b), we calculated the activation energies of Co deposition processes with different precursor flow rates based on the Arrhenius' equation. The activation energy is estimated to be 63.1 ± 1.2 kJ/mol on silicon substrates, which is in accordance with previous reports on thermal oxide substrates.[28,29]

To demonstrate the step coverage of our DLE-CVD Co films, we developed a parallel trench structure with an ultrahigh aspect ratio as a test platform. The fabrication of this trench structure is described in the Experimental Section, as well as schematically illustrated in Figure S3 in the Supporting Information. Co films were then deposited on the test structure by DLE-CVD at various temperatures at a constant precursor flow rate of 5 g/h. Cross-section SEM images were acquired to measure film thickness at different depths (as shown in Figure S4 in the Supporting Information), showing that our 200 °C film has over 95% step coverage at a 10:1 aspect ratio, and maintains 50% step coverage even at a 70:1 aspect ratio. The 230 and 260 °C films both have over 90% step coverage at a 10:1 aspect ratio, and maintain 50% step coverage at 60:1 and 35:1 aspect ratios, respectively.

In addition to high deposition rate and high conformality, low impurity level, for example, low carbon level, is also required for intermediate and global level interconnects because carbon content can decrease the conductivity of metal interconnects, thus increasing the energy consumption of overall device.[30,31] X-ray photoelectron spectra (XPS) of DLE-CVD Co samples deposited at different temperatures are provided in Figure 2d. All spectra are taken after 100 s of 100 eV Ar^+ sputtering to remove surface contamination. Substantial amounts of C (>5 at. %) are observed only in the samples deposited at above 290 °C. Samples deposited at temperatures up to 230 °C show less than about 1 at. % of C contamination. To estimate the impact of C content on DLE-CVD Co, we measured the conductivity of Co films with different C contents, which is discussed in the Supporting Information, Table S1. The results show that the resistivity substantially increased when the C content rose above 2 at. %, indicating that the DLE-CVD Co films deposited at lower than 230 °C (<1 at. % carbon shown by XPS) will be more promising to achieve better performance as interconnect materials. To further characterize these high-purity films with less than 1 at.

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% contaminants, a more sensitive method (e.g., APT) is needed to detect and quantify the impurities.

APT is an advanced characterization technique with ultrahigh atomic resolution for both composition and morphology. During an APT analysis, individual atoms are electrically evaporated one by one from the surface of a needle-shaped specimen, and analyzed by a 2D mass spectrometer to obtain their chemical and positional information at the same time.[32−34] Since APT offers chemical composition measurements at the atomic scale, this makes it a powerful tool to study our high-purity Co films with trace amounts of impurities, especially for the samples deposited at 200 and 230 °C.

As is shown in Figure 3a,b, we started the APT sample preparation by coating DLE-CVD Co films with precisely

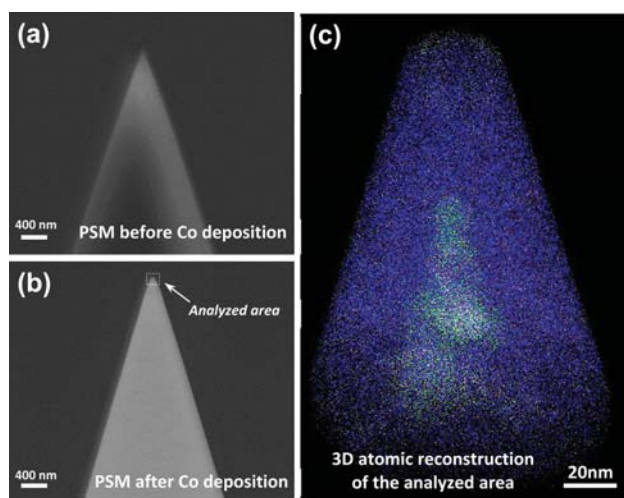

Figure 3. (a) SEM image of PSM before Co deposition; viewing angle is 30° from the cone axis. (b) SEM image of PSM after Co deposition; viewing angle is 30° from the cone axis. (c) 3D atomic reconstruction of the 200 °C DLE-CVD specimen, in which blue dots are Co (0.5% of all Co atoms displayed), gray dots are Si (50% displayed), green dots are O (100% displayed), orange dots are C (100% displayed), and red dots are N (100% displayed).

controlled thickness on silicon microtips presharpened to less than a 10 nm tip radius and 10° shank angle. Highly smooth and conformal Co films are observed on the microtips, as is demonstrated in Figure 3b. Laser-assisted APT analysis is then performed on the coated microtips at 40 K. Figure 3c is the 3D atomic reconstruction of the 200 °C DLE-CVD Co film in which the surface blue-colored dots are cobalt, green dots are oxygen, and gray dots are silicon. No obvious clustering or accumulation of impurities is observed, and most oxygen atoms exist only on the silicon tip surface, which is due to the UV-ozone cleaning before deposition to completely remove organic residues left from the lithography process. In Table 1, compositional data are collected from only the film part, excluding the atoms from the silicon tip and its surface. The sample deposited at 200 °C shows less than 0.8 at. % of each

Table 1. Compositional Data Acquired from Atom Probe Tomography

at. %	Co	C	N	O
200 °C	98.00 ± 0.20	0.76 ± 0.38	0.53 ± 0.28	0.71 ± 0.25
230 °C	96.80 ± 0.30	1.80 ± 0.35	0.33 ± 0.18	1.07 ± 0.30

contaminant (C, N, and O), and the sample deposited at 230 °C contains less than 1.8 at. % of these impurities. In APT reconstruction data, mild surface oxidations were observed, which we believe is due to air exposure after taking samples out of the deposition chamber for characterizations. This issue can be readily solved by installing tandem deposition setups and finish multiple metallization processes without an air break. With DLE-CVD design, tandem depositions are highly feasible because DLE-CVD can deliver multiple precursors solutions from different external precursor containers, and do depositions consecutively, which is another advantage of the DLE process.

For Cu liner/capping layer applications, it is important to develop nanocrystalline Co films to ensure smooth surface coverage of Cu wires. APT results demonstrate the ultra high purity and uniformity of our 200 °C DLE-CVD Co film, but do not provide information about microscopic surface morphology and crystallography. To obtain these characteristics, we performed transmission electron microscopy (TEM) and atomic force microscopy (AFM) imaging on the 200 °C sample. TEM image shown in Figure 4a reveals that the film is a nanocrystalline material with a grain size of around 10 nm. High-resolution imaging of lattice alignments at the grain boundary is included as the inset of Figure 4a. More high-resolution TEM images are also provided in the Supporting Information, Figure S5. Tapping-mode AFM surface scan (Figure 4b) shows a rms surface roughness of ∼0.9 nm, indicating that our DLE-CVD process produces highly smooth Co metal film.

X-ray diffraction (XRD) patterns of samples deposited at different temperatures (Figure 4c) reveal that, with lower deposition temperatures, the DLE-CVD Co tend to form smaller-sized nanocrystals. Figure 4d presents the electron diffraction (ED) pattern of the 200 °C DLE-CVD Co sample in which five major rings are observed. On the basis of the calculations in Table S2, ring 2 and ring 3 belong to hcp-Co (JCPDS 71-4239), ring 4 and ring 5 belong to fcc-Co (JCPDS 15-0806), and both phases contribute to the appearance of ring 1. Those results reveal that our DLE-CVD Co film is a mixed phase of fcc-Co and hcp Co, which is in accordance with our previous report.[23] We hypothesize that the competing growth between hcp and fcc induced lattice frustration and suppressed the growth of larger crystals, producing nanocrystalline films, which are favorable for Cu liner/capping applications.[35,36]

On the basis of the Co−Cu phase diagram, Co and Cu do not diffuse into each other at temperatures below 700 K, and only partially intermix at temperatures up to 1000 K from the thermodynamic point of view.[37] With high conformality, uniformity, and smoothness, our nanocrystalline Co films have appropriate properties to be used as an effective copper barrier and capping layer for Cu interconnects in microelectronics.[18,38] To evaluate the copper barrier performance of our DLE-CVD Co, capacitance−voltage ($C-V$) characteristics of $Cu/Co/SiO_2/Si$ and $Cu/SiO_2/Si$ systems were studied both before and after annealing at 600 °C. Fabrication details of the microcapacitors are described in the Experimental Section.

Figure 5a presents the $C-V$ curve of the $Cu/SiO_2/Si$ system, which shows a roughly 2 V shift toward the negative region after annealing. This phenomenon indicates that Cu ions diffused into the SiO_2 layer and formed positive charges.[9] However, as shown in Figure 5b, the $Cu/Co/SiO_2/Si$ system presented no observable shift of $C-V$ curve, indicating that Cu is effectively prevented from diffusing into SiO_2 by DLE-CVD Co at up to 600 °C. Since Co has much higher conductivity

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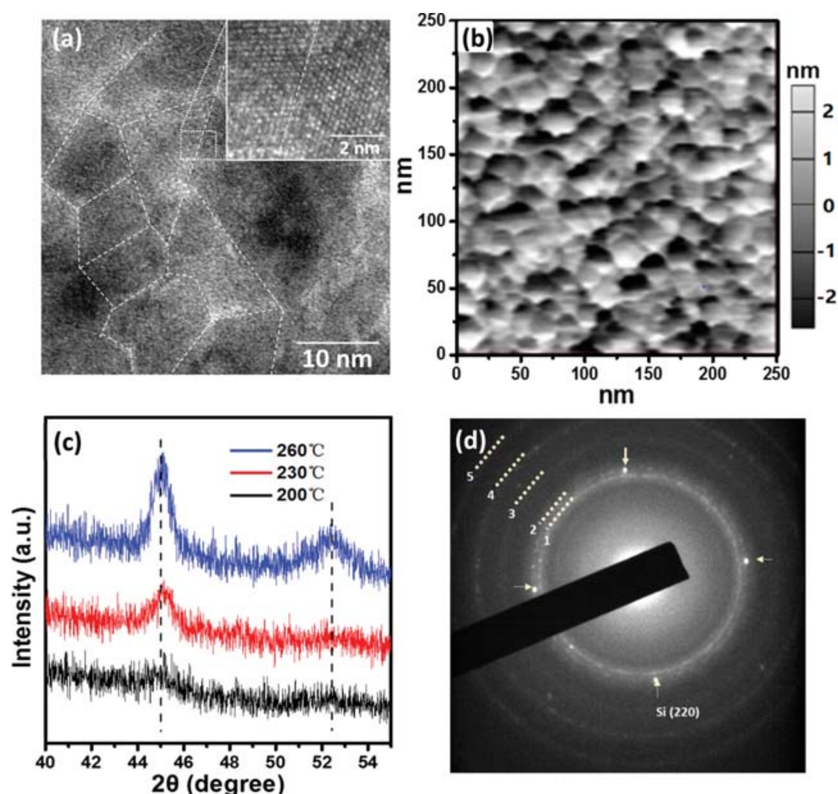

Figure 4. (a) TEM image showing the grain distribution of DLE-CVD Co deposited at 200 °C; (b) tapping-mode AFM image of DLE-CVD Co deposited at 200 °C; (c) XRD pattern of DLE-CVD Co deposited at different temperatures, showing peak broadening at lower temperatures due to the formation of nanocrystallines. (d) ED pattern of DLE-CVD Co deposited at 200 °C, in which the four marked dots belong to Si(220) reference.

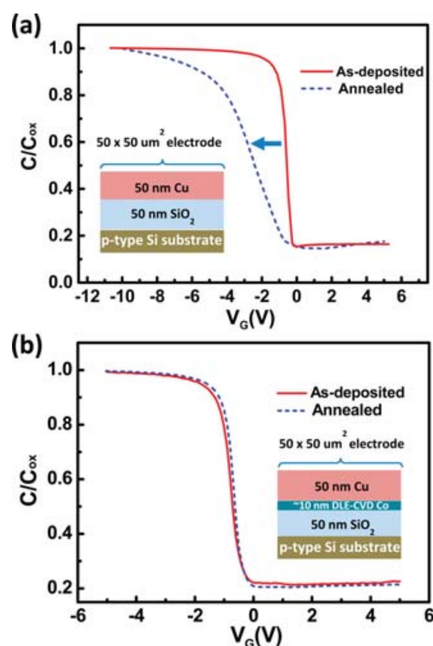

Figure 5. $C-V$ measurements on microcapacitor structures for the evaluation of Cu blocking capability. (a) Cu/SiO_2/Si system, showing ~2 V shift to the negative side; (b) Cu/Co/SiO_2/Si system, showing no observable shift of $C-V$ curve. All measurements started at positive 5 V and scanned from positive bias toward negative bias.

(1.60×10^7 S/m) than most metal nitrides, for example, TaN (0.76×10^6 S/m), the application of a Co liner may decrease the thickness of the barrier required for blocking Cu diffusion, while maintaining a low overall conductivity as close to pure Cu (5.96×10^7 S/m) as possible.[8,39,40] In this sense, the application of Co can potentially decrease energy consumption during electron transport in Cu interconnects.[15] Moreover, the strong adhesion at the Co/Cu interface can also substantially suppress surface electromigrations in Cu interconnects, thus increasing the lifetime of microelectronics devices.[41]

Taking advantage of the Cu barrier performance, smooth nanocrystallinity, and Cu surface adhesion of DLE-CVD Co, here we demonstrate that a nanocrystalline DLE-CVD Co film is an effective liner/capping material to three-dimensionally encapsulate Cu interconnects, thus enhancing their thermal stability and also suppressing potential electromigration. As a testing platform, nanoscale Cu wires were encapsulated all-around by DLE-CVD Co on thermal oxide substrates. In detail, a 10 nm thick Co film is first deposited onto a thermal oxide substrate, and then 500 nm wide Cu lines with a thickness of 60 nm were deposited onto the Co surface by standard e-beam lithography, metallization, and lift-off processes. Afterward, a final Co encapsulation layer was deposited onto the Cu surface by DLE-CVD. Meanwhile, as a control sample, bare Cu wires with no Co encapsulation layer were also deposited onto a thermal oxide substrate by the same method.

Figure 6a,b shows cross-section EDAX elemental mapping and SEM image of a Co-encapsulated Cu wire, demonstrating that the Co film is uniformly coated all around the Cu wire. After annealing at 600 °C for 2 h, the EDAX elemental mapping images in Figure 6c,d show that the Cu distribution is mostly maintained for the Cu wire sample encapsulated by DLE-CVD Co. However, as a control experiment, Figure 6e,f

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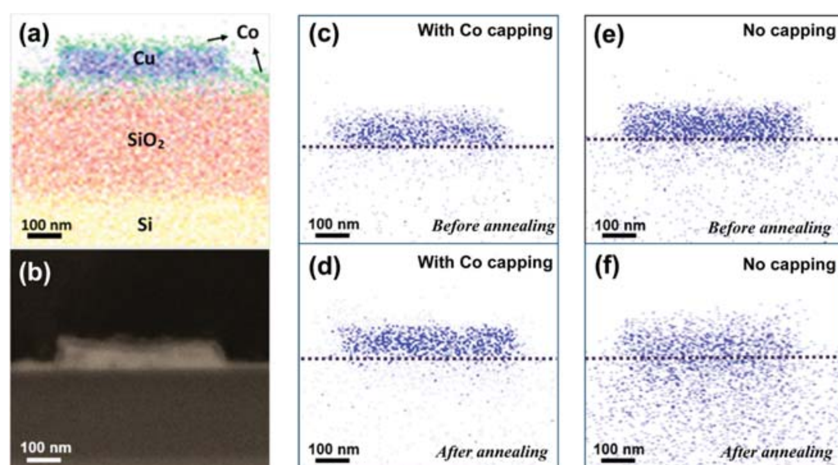

Figure 6. Demonstration of the application of DLE-CVD Co as an all-around encapsulation layer for Cu interconnects at nanoscales. (a) Cross-section EDAX elemental mapping of a Co-encapsulated Cu wire; (b) cross-section SEM image of a Co-encapsulated Cu wire; (c,d) cross-section Cu Kα_1 2D mapping of the Cu wires with Co encapsulation before and after annealing at 600 °C for 2 h, showing no obvious diffusion of Cu; (e,f) Cross-section Cu Kα_1 2D mapping of the Cu wires without any capping layer before and after annealing at 600 °C for 2 h, showing a substantial amount of Cu diffusion into SiO_2.

indicates that a substantial amount of Cu diffused into SiO_2 when Co encapsultion is not applied around a Cu wire since many more EDAX Cu counts were detected within the SiO_2 layer after annealing. This demonstration provides direct evidence that DLE-CVD Co nanocrystalline films are suitable as liner/capping layers that can substantially increase the reliability and lifetime of nanoscale Cu interconnects.

4. CONCLUSIONS

In this work, we demonstrated that DLE-CVD Co with highly controllable growth characteristics is a promising liner/capping layer for nanoscale Cu interconnects. Microscopic and crystallographic studies show that our DLE-CVD Co is composed of highly smooth nanocrystallines with a grain size of ∼10 nm and surface roughness rms of ∼0.9 nm. Less than 0.8 at. % of impurities was observed in APT analysis results for films deposited at 200 °C. On the basis of the nanoscale analysis of samples with and without Co encapsulation, it is proved that the diffusion of Cu is effectively blocked by DLE-CVD Co. Finally, with a nanoscale Cu line encapsulated all-around by Co as a proof-of-concept model, we demonstrate that our DLE-CVD Co encapsulation layer is able to substantially improve the thermal stability of nanoscale Cu interconnects. Also, taking advantage of the high conductivity and lower carrier MFP of Co, DLE-CVD Co encapsulation layers can potentially further decrease the power consumption of Cu interconnects with dimensions smaller than the MFP of Cu. This approach could allow the fabrication of Cu interconnects with higher efficiency in future microelectronic devices.

ASSOCIATED CONTENT

Supporting Information

The Supporting Information is available free of charge on the ACS Publications website at DOI: 10.1021/acsami.7b01327.

> Description of DLE-CVD system and Co precursor, fabrication process of test structures, step coverage evaluation method in a horizontal trench test structure, illustration of electrical test structures, and additional TEM and ED results (PDF)

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Author Contributions

The manuscript was written through contributions of all authors. All authors have given approval to the final version of the manuscript.

Notes

The authors declare no competing financial interest.

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