Chemical Vapor Deposition (CVD) of Manganese Self-Aligned Diffusion Barriers for Cu Interconnections in Microelectronics

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ABSTRACT

Barriers to prevent diffusion of copper, oxygen and water vapor were formed by CVD using a manganese precursor vapor that reacts with silica surfaces. The manganese metal penetrates only a few nanometers into the silica to make conformal amorphous manganese silicate layers. This $MnSi_xO_y$ was found to be an excellent barrier to the diffusion of Cu, O_2 and H_2O vapor. The adhesion strength of Cu to the $MnSi_xO_y$ was found to be sufficiently strong to satisfy the semiconductor industry requirements for interconnections in future microelectronic devices. CVD Mn dissolves into copper surfaces and then diffuses to increase adhesion to SiCNO capping layers.

INTRODUCTION

Copper (Cu) is now becoming the standard material for connecting transistors in microelectronic devices. However, transistors cannot function properly if Cu diffuses into them. Cu also reduces the resistance of the insulating material between the Cu wires. For both these reasons, Cu must be confined inside diffusion barriers that surround the Cu wires. Also, barriers to oxygen and water must separate these materials in the environment from the copper to prevent its oxidation. In current technology, the diffusion barriers are formed by sputtered tantalum nitride (TaN). Although TaN is an effective diffusion barrier, Cu does not adhere strongly to TaN. The adhesion of Cu to tantalum (Ta) metal is much stronger than to TaN, so Ta is sputtered on top of the TaN to enhance the durability of interconnect structures. Next in the process flow a thin Cu “seed” layer is sputtered, and then the trenches and holes are filled with Cu by electroplating.

As the dimensions of microelectronic circuits are being reduced, the non-conformal nature of sputtered barrier (TaN), adhesion (Ta) and seed (Cu) layers has caused problems. These layers are thicker near the top openings, so that the remaining openings are narrower at the top than lower inside the features. Then the electroplating process for Cu can form voids inside the features, which later can lead to failure of the interconnections. Another difficulty arises from roughness on the sidewalls of features, which may prevent deposition of the layers on recessed regions that are shielded from the line of sight to the sputtering target. If these areas are missing TaN, then Cu may diffuse out through these holes in the diffusion barrier. If Ta is missing from an area, then reliability may be reduced because of the reduced adhesion of the Cu to the TaN. If these areas are missing the Cu seed layer, then Cu electroplating will not take place on the oxidized surface of the exposed Ta,

producing voids in the Cu. Thus there is a need for methods to produce more conformal diffusion barriers, adhesion layers and seed layers. CVD and atomic layer deposition (ALD) are methods that can produce conformal diffusion barriers, adhesion layers and seed layers.[1]

Another problem with current diffusion barriers and adhesion layers is that TaN and Ta have a much higher resistivity than Cu. Thus by displacing Cu metal, they increase the resistance of interconnects. The time delay due to interconnects increases with their resistance, and thus the volume of barrier material should be minimized in order to form the fastest circuits. Ideally, a barrier should not occupy any of the volume reserved for Cu. Such a “zero-thickness barrier” can be realized by sputtering a manganese-Cu alloy, from which manganese diffuses into the surface of silica insulation at 450 ^{o}C.[2] The resulting self-aligned barrier layer of amorphous manganese silicate ($MnSi_xO_y$), just a few nm thick, remains part of the surface of the insulator, whose dimensions are not significantly changed by in-diffusion of the manganese. The resulting interconnects have lower resistance than ones made with conventional TaN barriers, and have proven to be even more durable as well.[3]

The self-aligned $MnSi_xO_y$ barriers start with sputtering of a Mn-Cu alloy, so they are still subject to the conformality problems of sputtered barriers. Voids in electroplated Cu may form under overhangs near the tops of features or inside rough areas on the sidewalls In this paper we propose a way to make conformal self-aligned $MnSi_xO_y$ barriers using CVD of manganese metal. We find that vapors of a manganese compound react with silica surfaces to form a thin amorphous layer of manganese silicate mainly within the surface of the silica. The $MnSi_xO_y$ layer is shown to be a good barrier against diffusion of Cu, O_2 and H_2O. CVD Mn also greatly increases the adhesion of copper to capping layers of SiCNO. The layer is completely conformal inside the surfaces of holes and trenches.

EXPERIMENTAL

The compound that serves as a precursor for the manganese is called bis(*N,N'*-diisopropylpentylamidinato)manganese(II), whose chemical formula is shown in Figure 1. The compound was synthesized by methods similar to those described previously.[4] It is a pale yellow crystalline solid that melts at about 60 ^{o}C to a clear liquid. For the CVD experiments, the manganese precursor was evaporated from the liquid in a bubbler at a temperature of 90 ^{o}C into a 60 sccm flow of highly purified nitrogen (concentrations of water and oxygen less than 10^{-9} of the N_2). The manganese precursor reacts immediately with oxygen or water to form a black material when it is exposed to air. The vapor pressure of the precursor is estimated to be around 0.1 mbar at 90 ^{o}C.

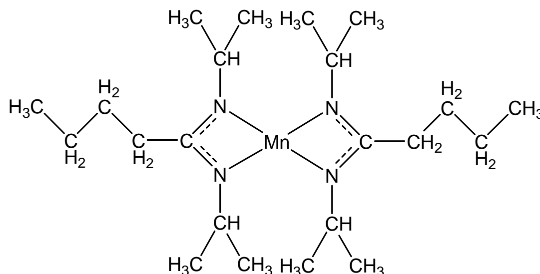


Figure 1. Chemical formula of bis(*N,N'*-diisopropylpentylamidinato)manganese(II).

The substrates of silica were either thermally oxidized silicon or silica deposited by ALD. The CVD was carried out in a hot-wall tube reactor (diameter 36 mm) within a tube furnace at temperatures between 200 and 400 ^oC and a total pressure of about 5 Torr. The amount of manganese deposited was measured by Rutherford backscattering spectroscopy (RBS). The $MnSi_xO_y$ formation was evaluated by cross-sectional high-resolution transmission electron microscopy (HRTEM). The effectiveness of the $MnSi_xO_y$ as a barrier to diffusion of Cu was tested in four ways: optical appearance, sheet resistance, Cu silicide formation and capacitance-voltage (CV) analysis of capacitors. For Cu diffusion tests, layers of SiO_2 8 nm thick were grown on HF-etched silicon wafers by ALD at 215 ^oC, followed by CVD Mn at 350 ^oC for 10 min, which formed 2.3 nm of Mn metal. Control samples of SiO_2 omitted the CVD Mn treatment. Then Cu layers about 200 nm thick were deposited on top of the CVD $MnSi_xO_y$ or SiO_2 layers. Anneals in a pure nitrogen atmosphere were carried out at temperatures of 400, 450 and 500 ^oC for one hour. For CV analysis, CVD Mn layer is deposited on 300 nm thermal SiO_2. Cu pad (500 μm diameter circle) is formed by thermal evaporator using shadow mask. CV was measured with a HP 4275A meter in a shielded probe station at room temperature. The Cu pad samples were used for Bias-Temperature Stress (BTS) test that was conducted at 250^oC under 1 MV/cm bias condition in Ar ambient. After this stress condition, CV was measured at room temperature.

RESULTS AND DISCUSSION

Thin Mn layers (2.3 nm) deposited on SiO_2 did not have any conductivity by 4-point probe (> 10^6 ohm/square). It may form $MnSi_xO_y$, which is an insulator, and any remaining metal Mn may be oxidized when the sample is taken out into the air for measurement. Thus, it is not clear from this measurement whether the CVD process deposited manganese metal or some insulating manganese compound. To confirm Mn metal deposition, CVD was carried out on substrates of Cu films 50 nm thick that had been evaporated onto SiO_2/Si substrates. The resulting structure was examined by cross-sectional HRTEM. Figure 2 shows that the CVD metal Mn diffused through the Cu layer and reacted with the SiO_2 to form an amorphous $MnSi_xO_y$ layer about 2~5 nm thick between the Cu and the SiO_2. The $MnSi_xO_y$ layer is thicker near grain boundaries in the Cu, along which Mn diffusion is faster. This result is evidence of Mn metal deposition.

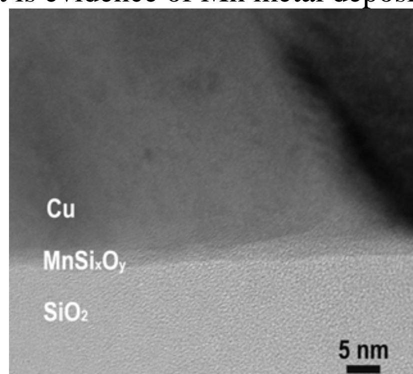


Figure 2. Cross-sectional HRTEM of CVD Mn / PVD Cu / SiO_2

The effectiveness of $MnSi_xO_y$ as a copper barrier was evaluated using a sample structure PVD Cu(200 nm)/CVD Mn (2.3 nm)/ALD SiO_2 (8 nm)/Si. A $MnSi_xO_y$ layer was formed between the Cu and ALD SiO_2 layers. The shiny Cu color and sheet resistances of these samples were unchanged by anneals in nitrogen at 400 or 450 ^oC. After a 500 ^oC anneal, the control sample, which does not have any $MnSi_xO_y$ layer, turned black and its sheet resistance increased by a factor of 200 because of massive diffusion of the Cu through the thin ALD SiO_2 into the silicon. The CVD Mn sample, by contrast, retained its shiny Cu color and increased its resistance only slightly.

To analyze for Cu diffusion, the remaining Cu layers were dissolved in nitric acid, and then the manganese silicate and silica were removed by dilute HF. The etched surfaces were then analyzed by an energy-dispersive X-ray spectrometer (EDX) and scanning electron micrographs (SEM). Figure 3 shows the SEM results after a 500 ^oC for 1 hr anneal. The few Cu-containing spots appear to be Cu silicide crystallites oriented by the crystal directions of the silicon. The control sample shows that the majority of its surface is covered by Cu silicide. The control sample showed a large Cu signal in EDX analysis that was stronger than the silicon signal, confirming that the thin ALD SiO_2 allowed diffusion of Cu. The CVD Mn-treated samples did not show Cu by large-area EDX.

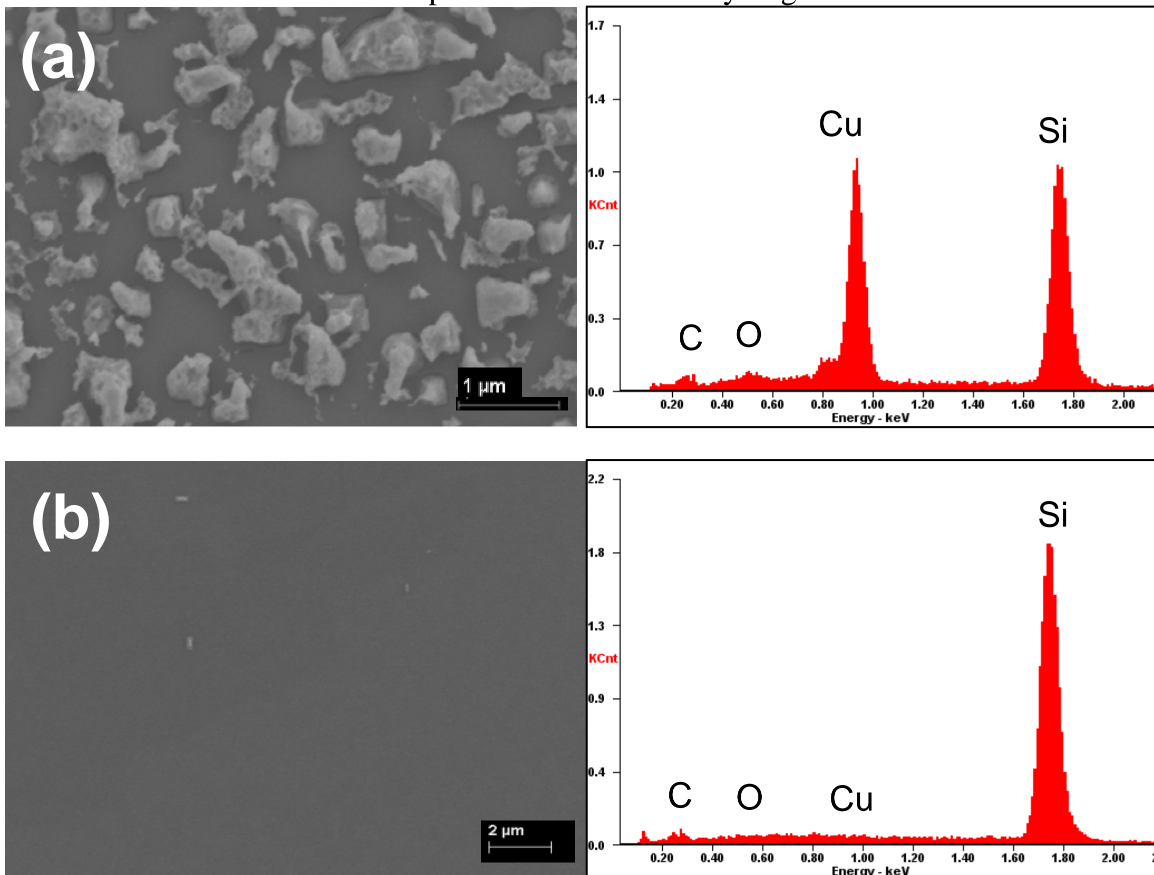


Figure 3. SEM of etched Si surface after annealing at 500 ^oC (a) with SiO_2 alone, and (b) with CVD $MnSi_xO_y$ on SiO_2.

An electrical test of barrier properties was carried out by patterning the Cu into capacitor electrodes. CV curves for samples annealed at 450 ^oC for 1 hr are shown in Figure 4. The large shift (-4.9 V) to negative voltages in the control sample is caused by positive Cu ions diffusing into the silica insulator.[6] In contrast, the silica protected by $MnSi_xO_y$ shows only a very small shift (- 0.1 V). This electrical test is more sensitive to diffusion of small amounts of Cu, than the other tests. These CV curves also demonstrate that the capacitance of the SiO_2 is not changed significantly by the CVD Mn treatment. Thus, we can expect this process is acceptable in low-k integration.

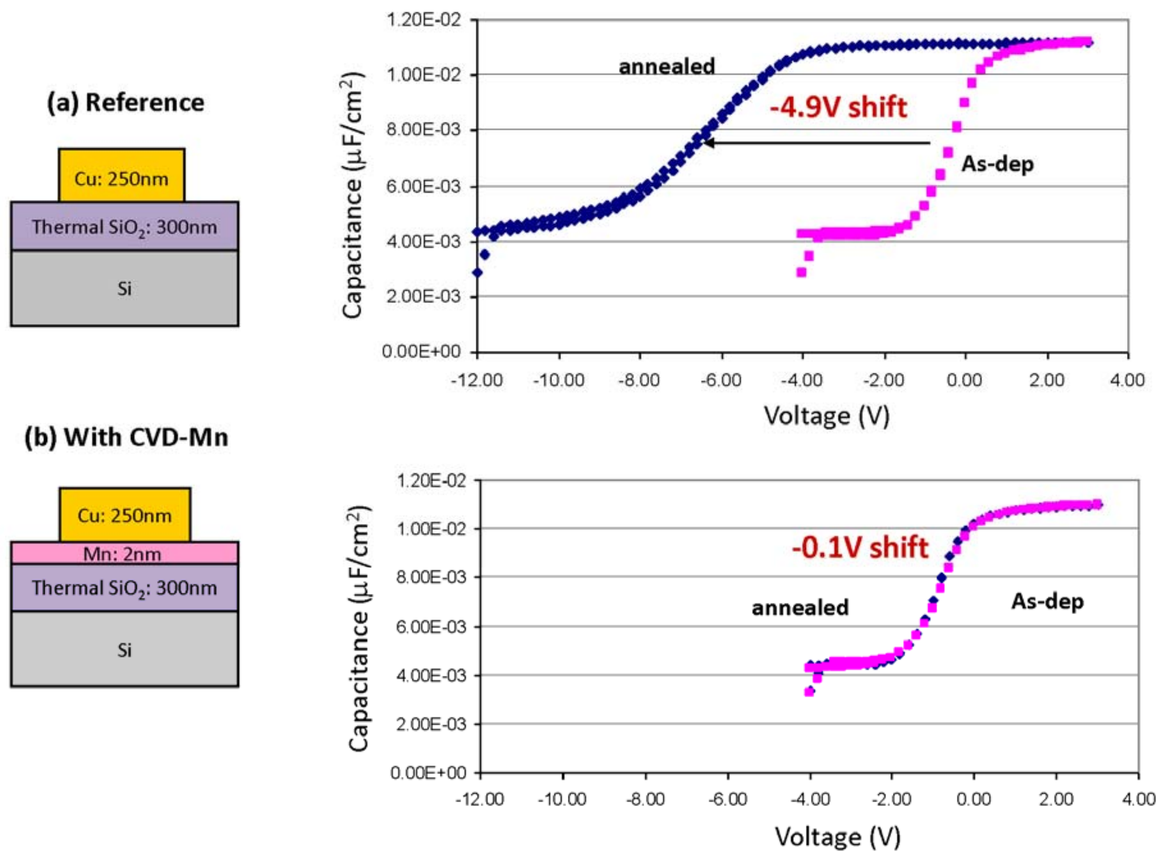


Figure 4. CV curves of samples before and after annealing at 450 ^oC (a) with SiO_2, and (b) with CVD $MnSi_xO_y$ on SiO_2.

Anneals of similar capacitors were also conducted under an applied voltage of 1 MV/cm at 250 ^oC. Bias temperature stress (BTS) test is more sensitive method for Cu diffusion into SiO_2, because Cu ion diffusion in the SiO_2 is accelerated by electric field.[6] BTS condition is closer to the environment of chip operation. Thus, BTS testing gives more relevant results for evaluating Cu diffusion barriers.[6] The control sample lost the capacitance behavior just after 2 min in the BTS condition, implying that a large amount of Cu diffused into the Si, so that the Si would not work as a semiconductor. However, the CVD Mn treated sample had no significant change in its CV curve (Figure 5). The results of this BTS test confirm the good Cu barrier properties of the $MnSi_xO_y$ layers.

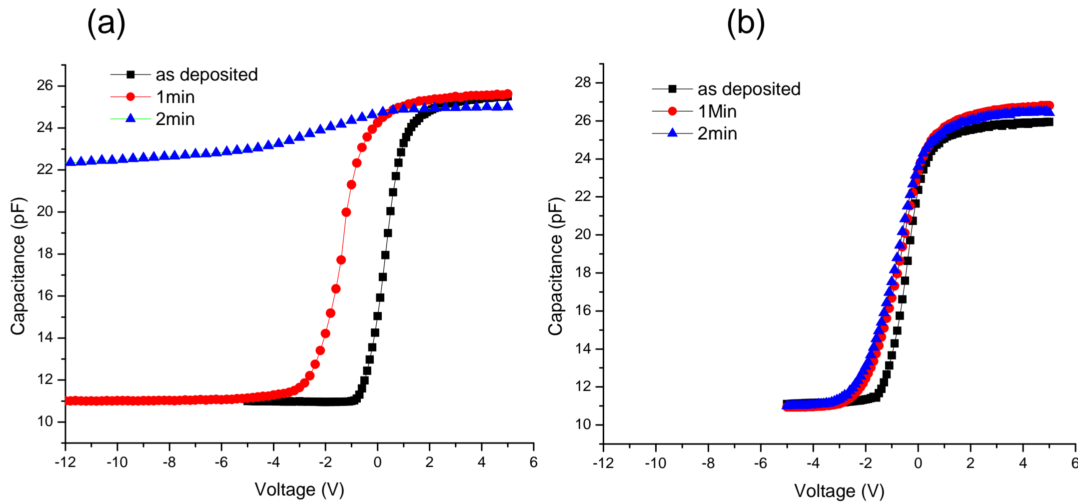
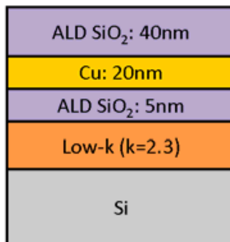


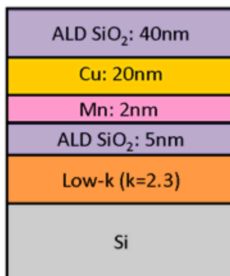
Figure 5. CV curves of samples before and after annealing at 250 ^oC under a 1 MV/cm field (a) with SiO_2, and (b) with CVD $MnSi_xO_y$ on SiO_2.

$MnSi_xO_y$ layers were also found to be good barriers to oxygen and water, which can corrode copper layers. To test how well the metal silicate layers protected copper, commercial low-k porous insulator layers from Applied Materials were coated with manganese as described above, followed by PVD copper. The top surface of the copper was protected with 40 nm of ALD silica.[7] The sample was cut into pieces to expose the edges of the low-k insulator so that oxygen or water vapor could diffuse into the low-k layer by the pathways shown in Fig. 6.

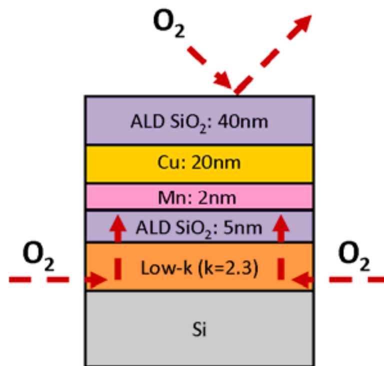
(a) Reference



(b) With CVD-Mn



Dry Oxidation Barrier Test
300°C, Dry Air, 24 Hours



Wet Oxidation Barrier Test
85°C, 85% Humidity, 24 Hours

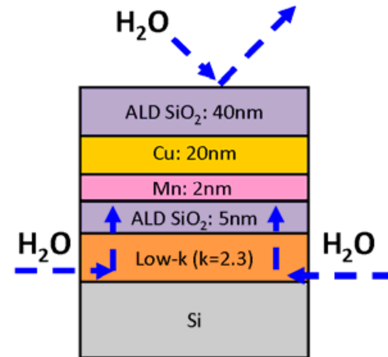


Figure 6. Sample structures and pathways for tests of $MnSi_xO_y$ as an oxidation barrier.

After exposure to dry air at 300 ^{o}C for 24 hours, the CVD-Mn-treated sample maintained its shiny copper color. A control sample without the CVD manganese treatment was corroded near its edges to dark copper oxide by the same exposure. This test shows that the manganese silicate layer is a good barrier to oxygen. Similar tests in a humid atmosphere (85% humidity at 85 ^{o}C for 24 hours) showed that the manganese silicate layer is a good barrier to water vapor. These exposures to water and oxygen also significantly increased the sheet resistance of the unprotected control copper layers, whereas the resistance of the Mn-protected copper layers remained nearly constant (Fig. 7.).

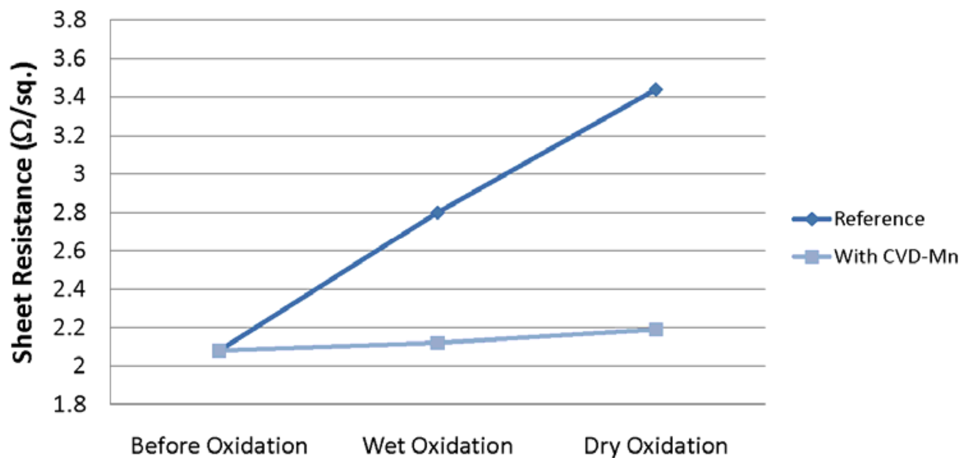


Figure 7. Sheet resistance of copper before and after oxidation.

The formation of the $MnSi_xO_y$ layer remarkably increased the adhesion of the Cu/SiO_2 interface, which failed the tape adhesion test prior to the CVD of Mn, but easily passed after the CVD of Mn. Adhesion strength was measured by 4-point bend tests.[5] The samples were prepared by CVD of Mn onto thermal SiO_2 on silicon wafers. Then CVD at 160 ^{o}C was used to form Cu oxynitride (CuON), which was then reduced to Cu metal by a hydrogen plasma at room temperature.[8] The adhesion energy was found to be 10.1 ± 1 J m^{-2}, which is higher than the value of 5 J m^{-2} that is considered to be sufficient for making durable interconnections.[9]

The CVD Mn process can also be used to strengthen the adhesion between copper and the commonly-used capping layers of SiCNO. To test this adhesion effect, 50 nm of copper was evaporated onto SiCNO layers (BLoK™, Applied Materials). The Cu showed very poor adhesion, with adhesion energy less than 3 J m^{-2}. Next, similar Cu/SiCNO layers were treated by CVD Mn at 350 ^{o}C for 10 minutes. This process increased the sheet resistance from 0.5 ohms/square to 1 ohm per square because of the manganese impurity in the copper. Then the structure was annealed for 1 hour at 400 ^{o}C in a nitrogen atmosphere. The sheet resistance then returned to 0.5 ohms per square because the manganese diffused to the surfaces or the interface. The out-diffusion of the manganese from the Cu film was confirmed by SIMS analysis. After the manganese treatment, the adhesion energy was remarkably increased to greater than 12 J m^{-2}, because manganese diffused to the interface, and made an interface layer. XPS confirmed the presence of manganese at both surfaces

created by delamination of the 4-point bend test sample. The exact compounds formed at the interface are not known.

This manganese metal diffusion process could be used to strengthen the bond between copper and the usual SiCNO capping layers. To do this, CVD Mn would be applied just after chemical-mechanical polishing, thereby dissolving Mn into the upper portions of the Cu below its polished surface. After SiCNO deposition, this dissolved Mn will diffuse up to the surface of the SiCNO and strengthen its bonding to the copper, probably increasing the electromigration lifetime.[10]

Complete conformality of the CVD CuON depositions in holes with aspect ratios up to 40:1 was confirmed by cross-sectional SEM studies.[8] Because the $MnSi_xO_y$ layers are too thin to image by SEM, the distribution of CVD $MnSi_xO_y$ was tested by Energy Dispersive Analysis by X-rays (EDAX) for Mn. The test substrates were holes in silicon with a very high aspect ratio of 52:1 and a native oxide surface with which the Mn precursor reacted. The results plotted in Fig. 8 show how the Mn content decreased with distance into the holes. At an aspect ratio of 3 (typical of interconnects), the step coverage is about 95 %. Even at the bottom of the very narrow holes (52 diameters deep) the amount of Mn is more than half of the amount at the top entrances to the holes.

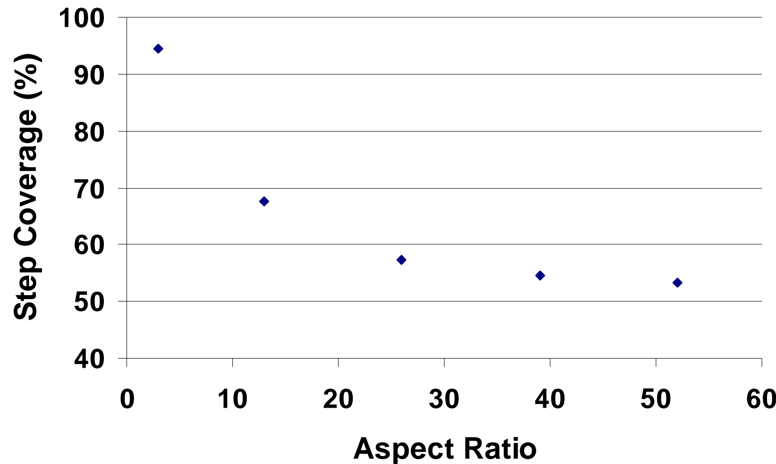


Figure 8. Distribution of CVD Mn down the length of a hole with aspect ratio 52:1.

This result shows that the Mn precursor has a fairly slow reaction with silica surfaces at 350 ^{o}C. Thus interconnect trenches and vias with typical aspect ratios less than 5:1 can be coated fairly uniformly with CVD $MnSi_xO_y$ at 350 ^{o}C. At lower temperatures, the surface reactions are expected to be slower, and the conformality should be even higher. Even when roughness is present on sidewalls, the CVD process should form a complete $MnSi_x$-O_y diffusion barrier without pinholes or gaps.

CONCLUSIONS

In summary, we presented a simple CVD method to make conformal self-aligned diffusion barriers of manganese silicate. This $MnSi_xO_y$ is an effective barrier to diffusion

of copper, oxygen and water. Because the $MnSi_xO_y$ is formed within the insulator, it does not decrease the volume available for Cu, as happens with conventional Ta/TaN barriers. Also, the CVD Mn dissolves into copper surfaces, such as at the tops of vias, so no resistive barrier exists between the tops of vias and the copper in the next higher level. The CVD process can also be used to strengthen the interfacial bonding between copper and a capping barrier layer of SiCNO. Thus more conductive and more durable interconnections are possible using the self-aligned $MnSi_xO_y$ barriers. The CVD Mn-CuON process should allow formation of conformal seed layers for void-free electroplating of Cu in even the narrowest interconnects.

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