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Sealing Porous Low-*k* Dielectrics with Silica

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The surface pores of a porous low-*k* dielectric layer were sealed by a smooth coating of silica just a few nanometers thick. Atomic layer deposition (ALD) of tungsten nitride (WN) onto the smooth silica surface provided a very thin (1.5 nm) barrier to the diffusion of copper. Without the silica sealing layer, ALD WN penetrated through the low-*k* dielectric. Strong adhesion was demonstrated for the structure Si/porous dielectric/SiO_2 /WN/Co/Cu, in which the top four layers were formed by ALD. This structure is stable to at least 400°C and is suitable for making narrow interconnects for future microelectronics.
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One of the strategies for increasing the speed of microelectronic circuits is to decrease the resistance-capacitance (RC) delay in the interconnections between the transistors. The resistance (R) has been reduced by replacing aluminum conductors with lower-resistance copper. The capacitance (C) was reduced by replacing the silica insulator (dielectric constant $k \sim 4$) by fluorinated silica glass (FSG, $k \sim 3.7$) and now organic-doped silica glass (OSG, $k \sim 2.8$). Further reductions in dielectric constant will require that the dielectric contain pores ($k \sim 1$ for the air in pores).[1] Several methods for making porous ultralow-*k* dielectrics have been demonstrated, using chemical vapor deposition (CVD) or spin-coating.[2]

Introducing pores into a dielectric poses several challenges for successful integration into microelectronic circuits. The mechanical strength of the dielectric is reduced by porosity, potentially leading to failure during chemical mechanical planarization (CMP) or during wire-bonding to the finished chip.[3] Moisture penetrating into a porous low-*k* material can increase its dielectric constant and leakage current, and reduce the voltage for dielectric breakdown.[4] Thus it is expected that porous low-*k* material in a microcircuit will need to be hermetically sealed from ambient moisture. Copper also diffuses readily through porous low-*k* materials, so an effective barrier is needed to confine the copper within the copper wires. The barrier to water and copper must be very thin (less than 4 nm by 2012[1]) so that it does not occupy volume needed for the current-carrying copper wires. If the barrier thickness is smaller than the largest pores, it becomes difficult to bridge the pores on the surface of the dielectric with a thin continuous barrier. Because barriers must be deposited inside trenches and vias with high aspect ratios, the barrier material will penetrate deeply into porous dielectrics. Indeed, atomic layer deposition (ALD) precursors can easily penetrate entirely through porous dielectrics, causing an electrical short circuit through the insulator.[5]

Sealing of porous dielectrics by plasma treatment has been proposed to provide a continuous surface on which thin barriers could be deposited.[6,7] Although a plasma treatment can be applied to the upper surface of a porous dielectric, it is not clear that plasma particles can be projected successfully into increasingly narrow trenches and vias to seal the pores in their side-walls.

In this paper, we propose and demonstrate a pore-sealing method based on the catalytic growth of silica in the pores near the surface of a porous low-*k* dielectric. A small (submonolayer) dose of aluminum catalyst is supplied to the surface of the dielectric and its pores close to its surface, as illustrated in Fig. 1. Then a single dose of vapor of tris(tert-butoxy)silanol is exposed to the surface, resulting in the selective growth of silica only on the catalyst-covered parts of the surface.[8] Experimental conditions during the silica deposition were chosen to provide a thickness of silica sufficient to close the largest pores. The maximum depth to which the pores are filled by the silica is controlled by the depth to which the aluminum catalyst is placed, and this depth can be controlled in a well-understood way by adjusting the experimental ALD conditions during the deposition of the catalyst.[9]

Experimental

The aluminum catalyst was formed by exposure of the dielectric to vapor of trimethylaluminum (TMA), the source of which is solid TMA in a stainless steel container at −8°C. The silica was formed from the vapor of tris(*tert*-butoxy)silanol (TBOS) kept in a stainless steel container heated in an oven to 115°C, at which temperature it is a liquid (melting point 65°C). The home-made ALD apparatus has been described previously.[7,10] Porous low-*k* dielectric films (JSR LKD-6103), spin-coated to a thickness of 0.4 μm on a silicon wafer, were used as substrates. These films have dielectric constant about 2 and mean pore diameter 5.5 nm. Test depositions were also done on dynamic random access memory (DRAM) trench capacitor structures having narrow holes 8 μm deep and ~0.17 μm in diameter etched in silicon. The samples were placed on a half-cylinder substrate holder inside a tube furnace (inner diameter 3.7 cm) heated to 300°C for 1 h in flowing nitrogen to desorb moisture from the low-*k* material.

Pore-sealing was accomplished by only one ALD cycle on the substrates at 300°C. To seal the surfaces of the pores without filling the interior of the porous low-*k* material, we chose ALD conditions that would only coat a short distance into a hole or pore. First, one dose (0.22 micromoles) of TMA vapor was released by opening a valve for 1 s. This TMA vapor dose was carried by 40 sccm nitrogen gas flowing through the deposition zone into a vacuum pump that maintained a pressure of 0.3 mbar, giving an exposure of about 2×10^3 Langmuirs. This exposure is much smaller than the amount we used previously[8] to coat conformally the entire length of holes with high aspect ratios. The carrier gas flow continued for 15 s to purge the chamber of unreacted TMA. Then, one dose (70 micromoles) of TBOS was released into the flowing carrier gas by opening a valve for 2 s, providing an exposure of about 7×10^5 Langmuirs. These conditions deposited ~4 nm of silica, as measured on a witness substrate of silicon by a Woolam spectroscopic ellipsometer. Dielectric constants were measured for the porous low-*k* dielectric films before and after pore-sealing, by sputtering platinum capacitor electrodes through a shadow mask.

Deposition of tungsten nitride was done by ALD using cycles of alternating bis(dimethylamido)bis(*tert*-butylimido)tungsten(VI) vapor and ammonia gas, to deposit WN on the silica-coated substrates heated to 350°C.[11,12] Then, Rutherford backscattering (RBS) was used to test whether the WN remained on the surface or penetrated into the dielectric.

ALD cobalt films were grown on top of WN films by alternating doses of bis(*N*,*N*′-diisopropylacetamidinato)Co(II)[13] vapor and H_2 at a substrate temperature of 300°C.[14] Copper films were formed by ALD from (*N*,*N*′-diisopropylacetamidinato)Cu(I)[13] dimer vapor and H_2 exposed to a cobalt-covered surface at 190°C.[14]

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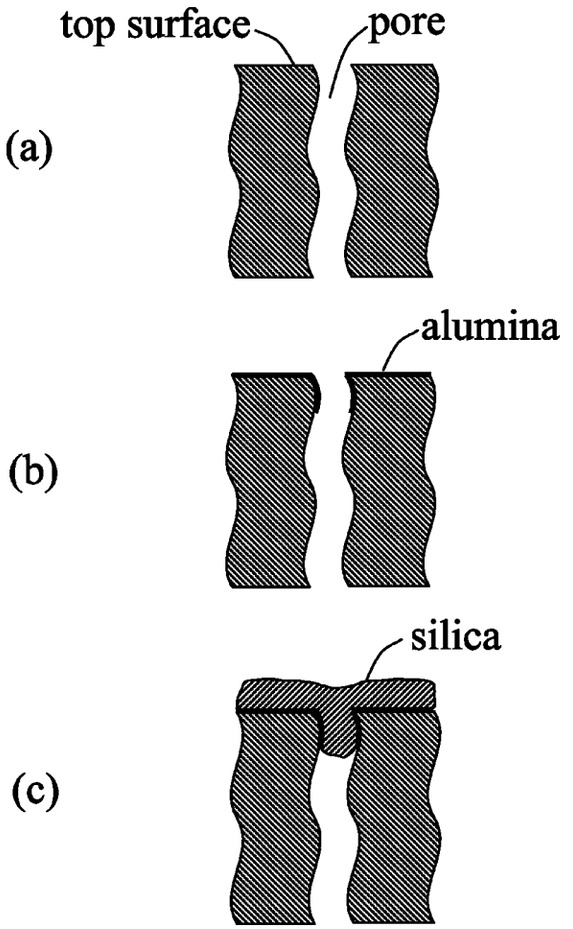

Figure 1. Schematic cross-section near the surface a porous low-*k* materal. (a) Uncoated, (b) top surface and top of pore coated with about one-third of a monolayer of alumina catalyst, and (c) top of pore sealed with silica grown catalytically on the alumina.

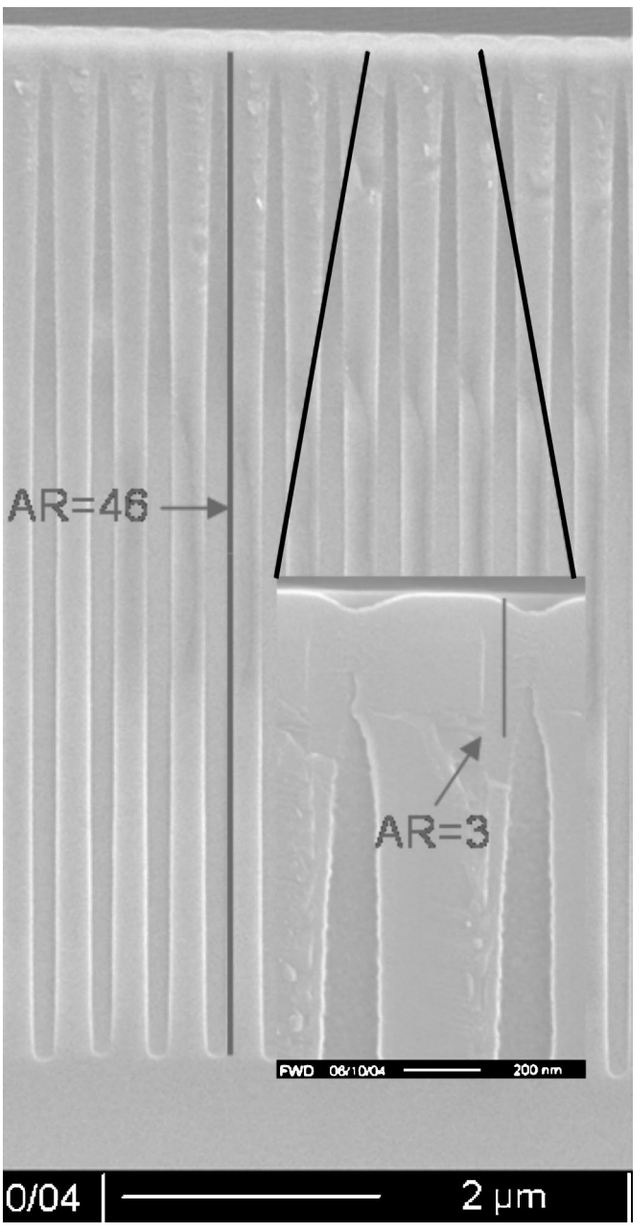

Figure 2. SEM of a cross-section of holes with aspect ratio 46 whose tops are sealed with 100 nm of ALD silica nanolaminate. The inset in the lower right shows a higher-magnification image of the sealed tops of two holes.

Results and Discussion

A test substrate of planar silicon was found by ellipsometry to have a silica layer ~4 nm thick after one ALD cycle described above. To test how far this coating would extend into holes, we used silicon etched with narrow holes (aspect ratio 46) as a test substrate. To make a coating thick enough to image easily by scanning electron microscopy (SEM), we used 25 ALD cycles to form a coating ~100 nm thick on this test substrate. The results in Fig. 2 show that the coating only extended into the holes to a depth of about three diameters. Because of the relatively low exposure to the TMA vapor, the penetration of the aluminum catalyst was limited to less than about a 3 to 1 aspect ratio. Only in this top portion of hole did the silanol vapor meet the previously deposited aluminum catalyst necessary for the growth of silica. Of course these DRAM holes are about a hundred times larger in diameter than the pores in the porous low-*k* dielectric. However, these larger holes are a faithful large-scale model for what happens in the smaller low-*k* pores because both of their diameters are much smaller than the mean free path (hundreds of microns) inside the reactor atmosphere during deposition. Thus there are no collisions between gas molecules inside the holes or pores, and transport inside them is by molecular diffusion. Therefore, the only important parameter governing the shape of the deposit is the aspect ratio, not the absolute sizes of the holes.

To see if the small pores in the low-*k* material were sealed by one cycle of ALD silica, 100 cycles of ALD WN were subsequently deposited on a silica-coated low-*k* sample, giving a WN film ~10 nm thick. For comparison in the same run, WN was deposited on an uncoated sample of porous low-*k* material. Portions of the RBS spectra for these two samples are shown in Fig. 3. The tungsten RBS peak for the unsealed low-*k* sample shows a long tail extending to lower energies, showing that the WN had penetrated into the pores of the unsealed low-*k* sample. Modeling of this RBS spectrum indicated that the WN had penetrated completely through the 0.4 μm thick unsealed low-*k* material. In contrast, the tungsten peak for the sealed sample is very sharp, demonstrating that the WN remained on the surface and did not penetrate into the pores. Control experiments (not shown) showed that the RBS peak shape from WN deposited on nonporous thermally grown silica matched the RBS peak shape from the sealed surface. We conclude that the deposited silica thickness (4 nm) is greater than the maximum pore radius for the pores in this sample. This result is consistent with the mean pore

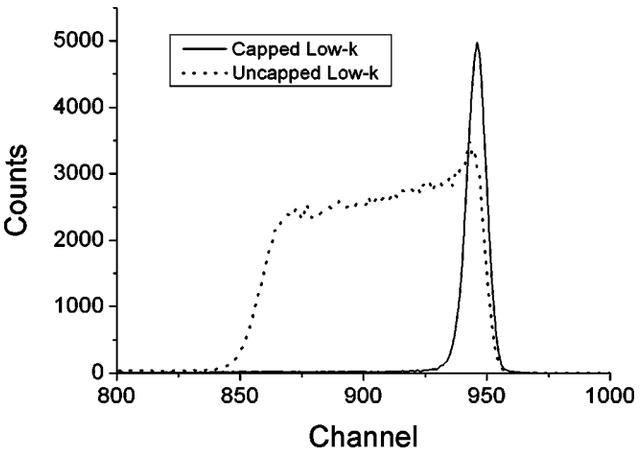

Figure 3. The tungsten region of the RBS of tungsten nitride deposited on porous low-*k* dielectric (a) sealed with ALD silica (solid line) and (b) unsealed (dotted line).

radius of 2.75 nm estimated by nitrogen adsorption for this low-*k* material. The dielectric constant of the low-*k* material was not changed by the sealing process, to within the accuracy ($\pm 2\%$) of the dielectric measurement.

Samples with the structure Si/low-*k*/silica/WN/Co/Cu were made to simulate a possible interconnect barrier/seed layer made entirely by ALD. The WN serves as a barrier to diffusion of copper. The cobalt layer increases the adhesion strength and the nucleation density of the copper. 15 cycles of ALD tungsten nitride deposited ~1.5 nm of WN. 50 cycles of ALD cobalt produced a Co film ~1.0 nm thick. 100 cycles of ALD copper formed a Cu film ~10 nm thick. Tape-pull tests showed that this multilayer stack has good adhesion. Samples were annealed at 400°C for 30 min in 5% H_2/95%N_2 at atmospheric pressure. SEM showed no agglomeration of the copper film and RBS showed no diffusion of copper into the low-*k* material.

Conclusions

ALD processes have been used to seal porous low-*k* material with silica, and to add a tungsten nitride diffusion barrier, a cobalt adhesion layer, and a copper seed layer. This structure provides a thin, highly conformal, strongly adherent barrier and seed layer for further deposition of copper for interconnects.

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