Self-Aligned 40 nm Channel Carbon Nanotube Field-Effect Transistors With Subthreshold Swings Down to 70mV/decade

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Much progress has been made in recent years in the fabrication and understanding of the operations of Single-walled carbon nanotube (SWNT) field effect transistors (FETs). [1-4] Nevertheless, it remains a challenge to develop highly scaled device structures for nanotube transistors and push to the performance limit of these molecular materials. The purpose of this work is to fabricate highly scaled SWNT field effect transistors (FETs) and approach the performance limit of carbon nanotube FETs.

Our main result here is successful fabrication of nearly ballistic p-channel SWNT FETs with 40 nm channel lengths, self aligned source (S), drain (D) and gate electrodes, palladium S and D contacts with low contact resistance and HfO_2 high-κ dielectric gate insulators. The current work builds upon our recent demonstration of self-aligned 50 nm channel SWNT FETs,[3] and has achieved several new and important milestones for nanotube transistors including, (1) Further gate length scaling. (2) Small diameter SWNTs (d~1.5nm) with large band gaps are used to obtain SWNT-FETs with $I_{ON}/I_{OFF} > 10^4$ and reduced ambipolar conduction at a bias of V_{ds}=0.3 V. Diameter dependent SWNT-FET performance is investigated. (3) Subthreshold swings down to 70mV/decade at V_{ds}=0.3 V is achieved by enhancing the gate capacitance.

Fabrication of SWNT FETs started with patterned chemical vapor deposition (CVD) of nanotubes on SiO_2 (thickness ~ 500 nm)/Si substrates (Fig. 1). Our final devices consisted of L~40 nm long SWNTs between palladium S and D contacts, t_{ox}=8 nm thick HfO_2 (κ~15) gate insulator formed on top of SWNTs by atomic layer deposition (ALD) at 90 ºC and top Al gate

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electrodes (Fig. 1a&b). The S, D and gate were self-aligned without overlapping or significant gaps between them (Fig. 1a). This was made possible by first forming the gate stack (by ALD of high-κ at 90ºC followed by Al evaporation on PMMA patterned substrates and then liftoff of PMMA). We then used the gate stack with native Al_2O_3 (4-8 nm thick) as a mask for depositing thin Pd/Au (~2/5 nm) S and D electrodes (Fig. 1a&b). The insulating Al_2O_3 film on the Al gate and the directional deposition of thin Pd ensured electrical insulation between G, S and D. Details of the fabrication were as described recently.[3]

Fig. 1c&d shows the characteristics of a L~40 nm SWNT FET with a small diameter of d~1.5 nm. The maximum current reached at V_{ds}=0.3 V is I_{max} ~ 10 μA with $I_{max}/I_{min}=10^4$ and no appreciable ambipolar n-channel conduction. Compared to larger diameter SWNT FETs (d~2 nm, Fig. 3), the small diameter FET exhibits lower I_{max} (~10 μA vs. ~20 μA) mainly due to positive Schottky barriers existing between Pd and small diameter tubes. The small diameter nanotube FETs are advantageous in 10 times higher I_{max}/I_{min} and significantly lower n-channel leakage currents, due to the larger band-gap of the nanotubes (E_g~1/d~0.6eV for d=1.5 nm). Thus, our current results show that with Pd S/D contacts, SWNTs with d~1.5 nm (E_g~1/d~0.6eV) can afford high performance FETs with high ON/OFF ratios without large compromise on I_{max}. Future work should focus on developing new contact strategies for even smaller diameter (~ 1nm, E_g=0.88eV) SWNTs to further optimize both I_{max} and I_{max}/I_{min}. Note that for the L=40 nm SWNT channels, nearly ballistic transport is achieved to afford high I_{max} up to ~20 μA at relatively low V_{ds}=0.3V. The mean free path for optical phonon scattering under high biases (>0.2V) is ~ 10-15 nm, only slightly below the channel length.

Our current self-aligned SWNT FETs exhibit subthreshold swings down to S~70mV/decade at V_{ds}=0.3 V (Fig. 3). This is a significant improvement over the recent similar

devices (s~110 mV/decade in ref. 3) simply owing to the thicker SiO_2 (500 nm vs. 10 nm) substrate used in the current work that allows for enhanced top-gate electrostatic control over the nanotube channel. Further improvement of S is currently being pursued by using thinner HfO_2 high-κ gate dielectrics (reducing t_{ox}=8 nm to t_{ox}=5 nm and below).

In summary, we have fabricated 40 nm channel nearly ballistic SWNT FETs with self-aligned geometry. The results represent important steps forward in nanotube electronics. Future work will include further scaling of these molecular transistors, ohmic contacts to small diameter nanotubes and n-channel self-aligned SWNT FETs.

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References:

1. A. Javey, et al. , *Nature* 424 , 654-657 (2003).

2. A. Javey *et al.* , *Nature Materials* 1 , 241 - 246 (2002).

3. A. Javey, et al. ,Nano Lett., ASAP article.

4. S. Wind, et al, *Appl. Phys. Lett.*, *80*, 3817-3819 (2002).

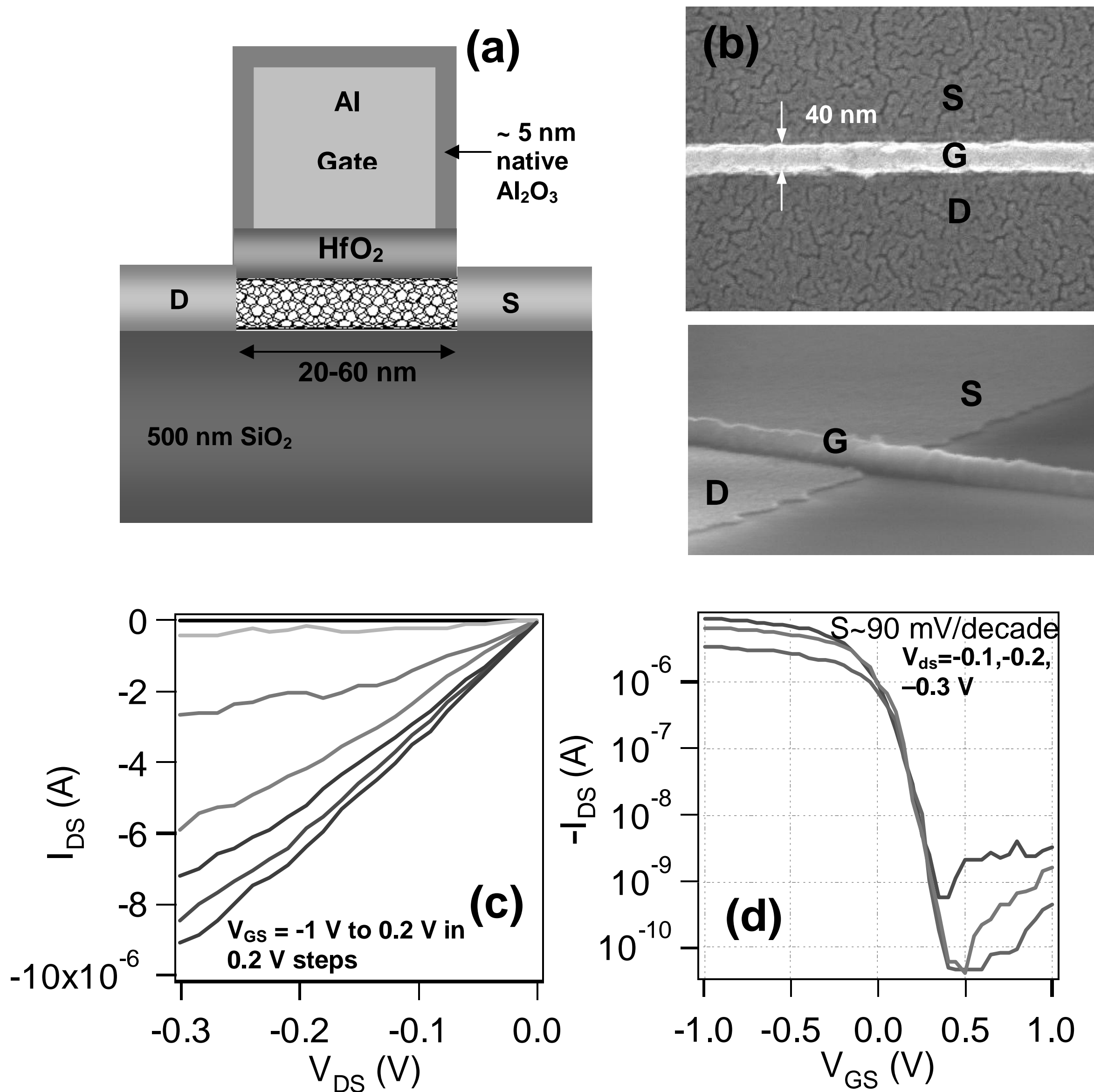

FIG. 1 Self-aligned 40 nm long SWNT FETs with tube diameter d~1.5 nm. (a) Side-view schematic of a device. (b) Scanning electron microscopy (SEM) images of a device with 40 nm gate length. The nanotube beneath the electrodes is not visible in the SEM images. (c) Current vs. top-gate voltage (I_{DS}-V_G) for a device with a L~40 nm and d~1.5 nm SWNT at different biases (V_{DS}). PMMA passivation was used for the measurements. (d) I_{DS}-V_{DS} characteristics of the same device.

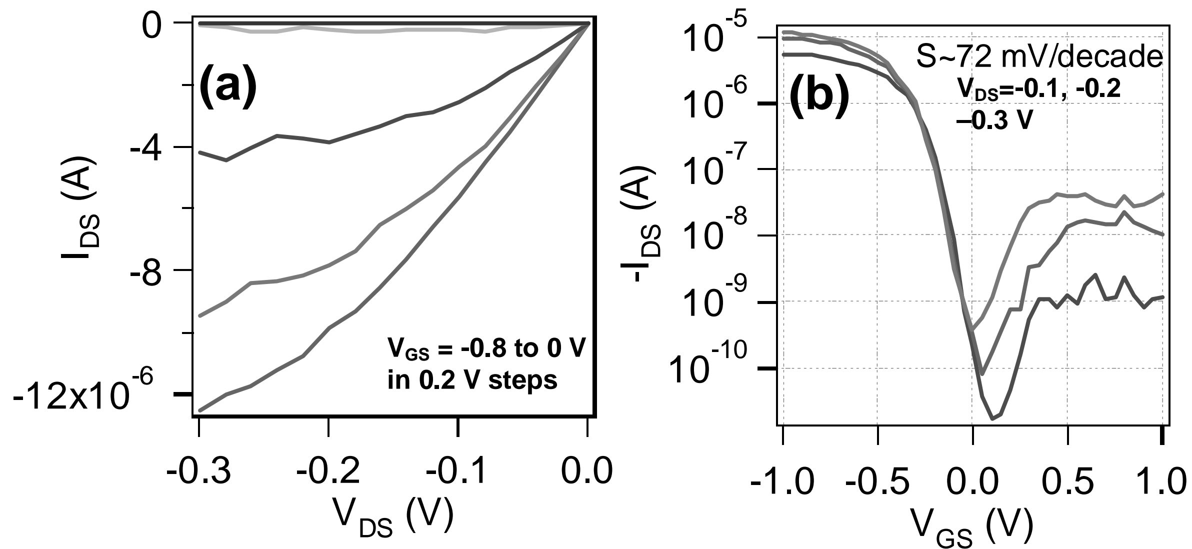

FIG. 2 A 40 nm channel self-aligned SWNT FET with tube diameter ~ 1.7 nm. (a) I_{DS}-V_{DS} of the device at different gate biases V_{GS}. (b) I_{DS}-V_{GS} characteristics of the same device.

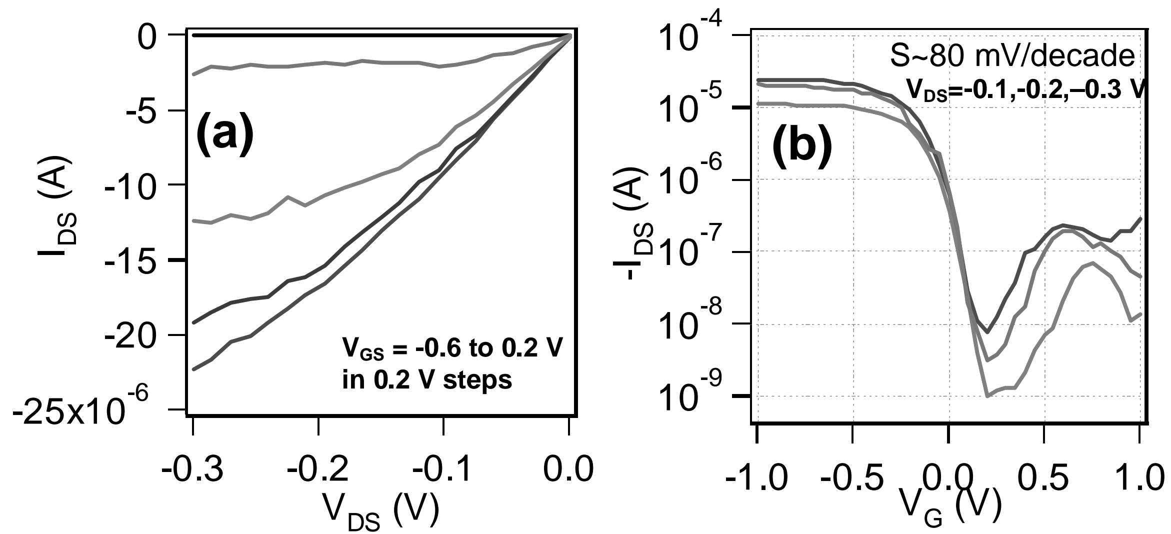

FIG. 3 A 40 nm channel self-aligned SWNT-FET with tube diameter ~ 2 nm. (a) I_{DS}-V_{DS} of the device at different gate biases V_{GS}. (b) I_{DS}-V_{GS} characteristics of the same device.