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# Advanced Atomic Layer Deposition and Epitaxy Processes

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# Single-crystal oxide insulators grown epitaxially on GaAs, Ge and GaN by ALE

## Outline

Atomic Layer Epitaxy (ALE)

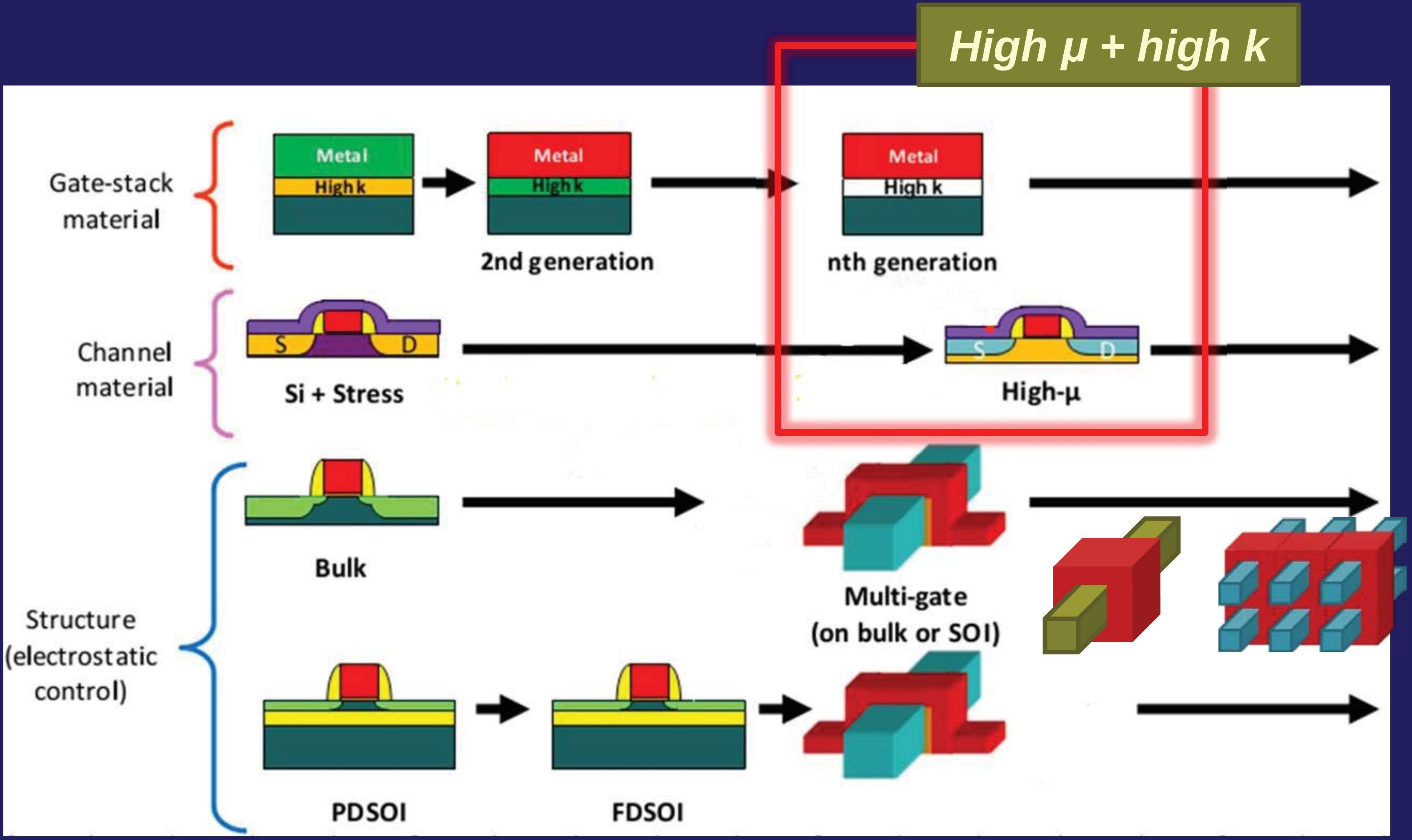
ALE of single-crystal $La_2O_3$ on GaAs(111)

CMOS circuits with $La_2O_3$ on GaAs(111)

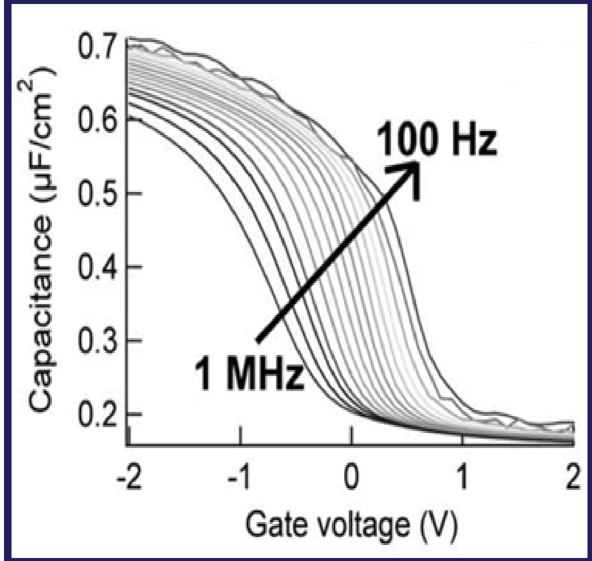
ALE of single-crystal $La_2O_3$ on Ge(111)

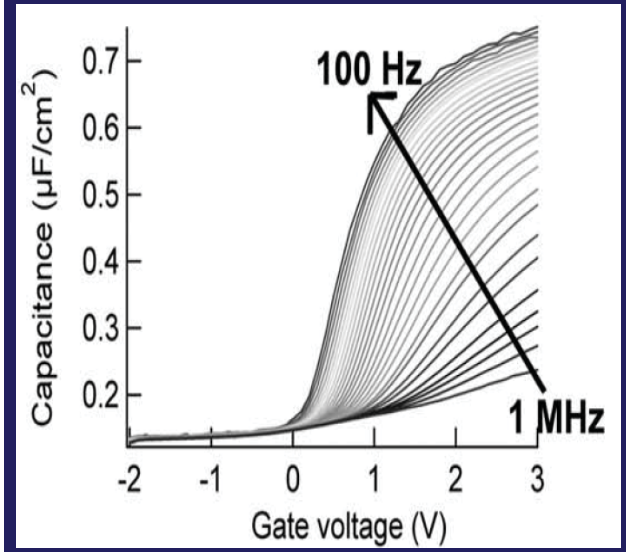
ALE of single-crystal (Mg,Ca)O on GaN(0001)

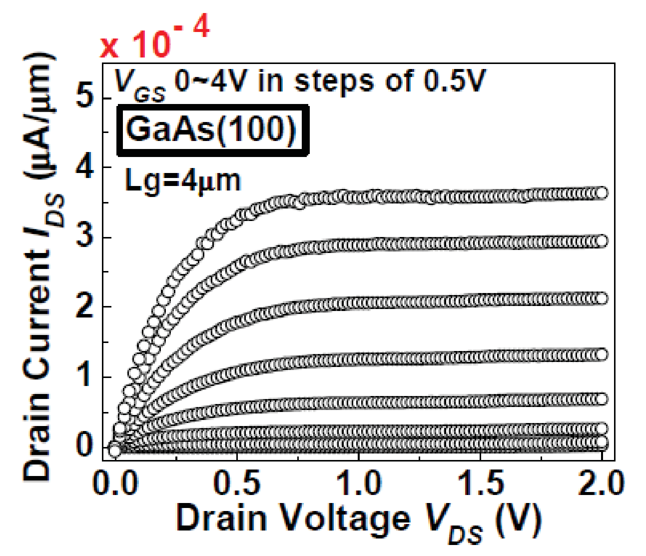
# ITRS roadmap



# GaAs has Many Traps at Oxide Interfaces







=> very large frequency dispersion

=> very low drive currents

**~$10^{13}$ cm$^{-2}$ traps at GaAs interface with oxides**

**<$10^{11}$ cm$^{-2}$ traps at Si/SiO$_2$ interface**

**=> GaAs MOS transistors are much poorer than Si**

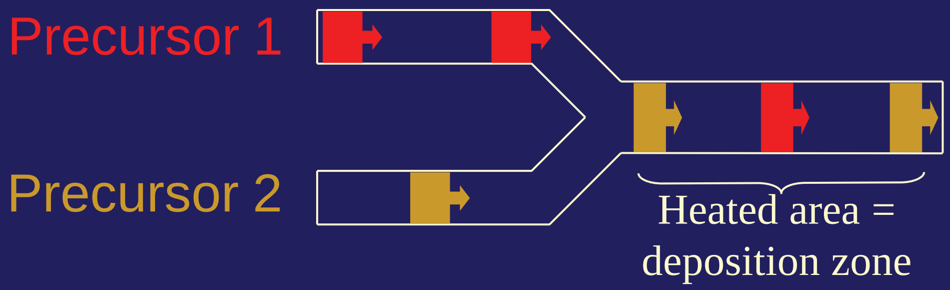
**Solution: epitaxial single-crystal La$_2$O$_3$ on GaAs**

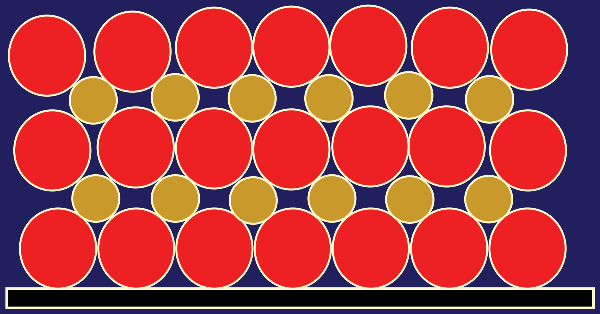
**⇒ ~$10^{11}$ cm$^{-2}$ traps at GaAs/La$_2$O$_3$ interface**

**⇒ First CMOS transistors ever made on GaAs**

# Atomic Layer Epitaxy (ALE)

Sequential, self-limiting surface reactions make alternating layers:



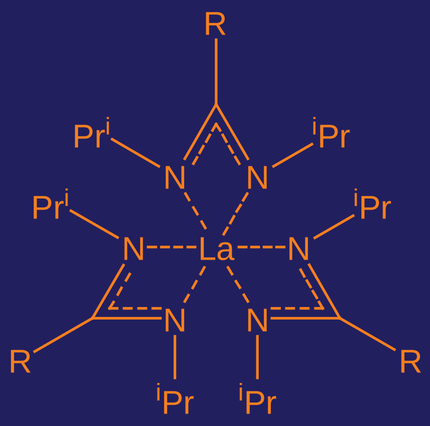


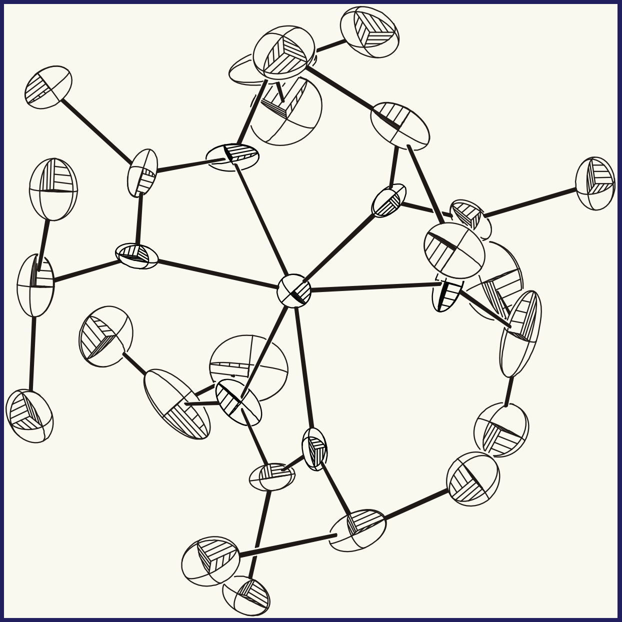
Benefits of ALE:

- High-quality epitaxial interfaces with few traps
- Atomic level of control over film composition
  ⇒nanolaminates and multi-component materials
- Uniform thickness over large areas and inside narrow holes
- Smooth surfaces
- High density and few defects or pinholes
- Low deposition temperatures (for very reactive precursors)
- Pure films (for suitably reactive precursors)
- Full-wafer semiconductor-grade production equipment available

# Amidinate Precursors for Trivalent Metals

**La**, Ce, Pr, Nd, Sm, Eu, Gd, Tb, Dy,
Ho, Er, Tm, Yb, Lu, **Y**, Sc, In, Ru, Ti



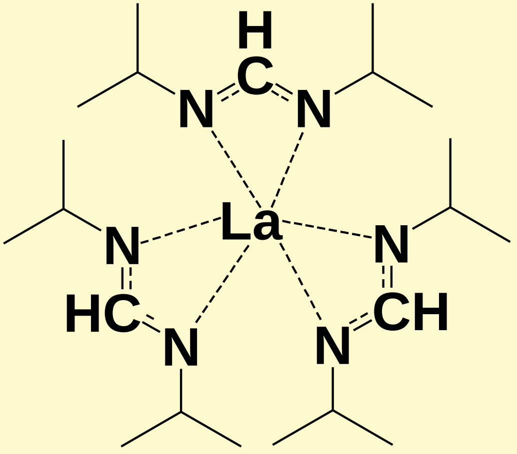


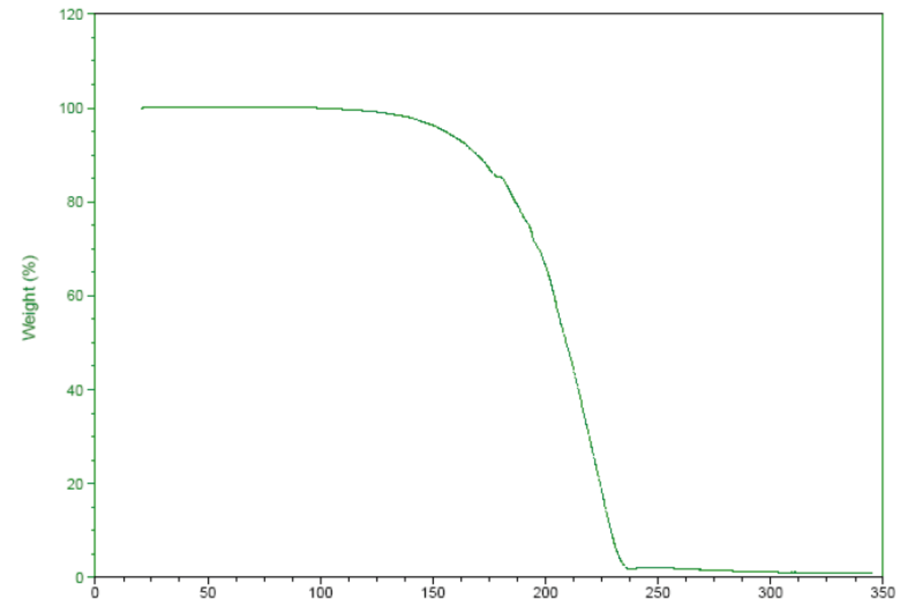
R = H (formamidinate, fmd)
R = $CH_3$ (acetamidinate, amd)

Now produced commercially by the Dow Chemical Company

# Vaporization of Lanthanum Amidinate Precursor

tris(N,N’-diisopropyl-formamidinato)lanthanum
$La((^{i}Pr_2N)_2CH)_3$
abbreviated $La(fmd)_3$





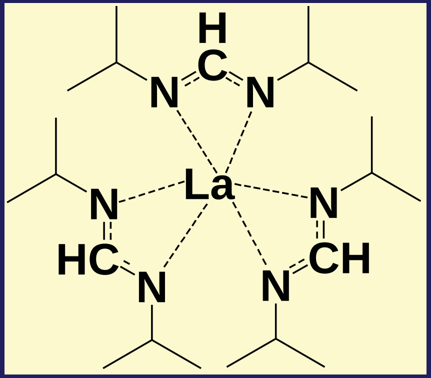
Most volatile lanthanum compound known

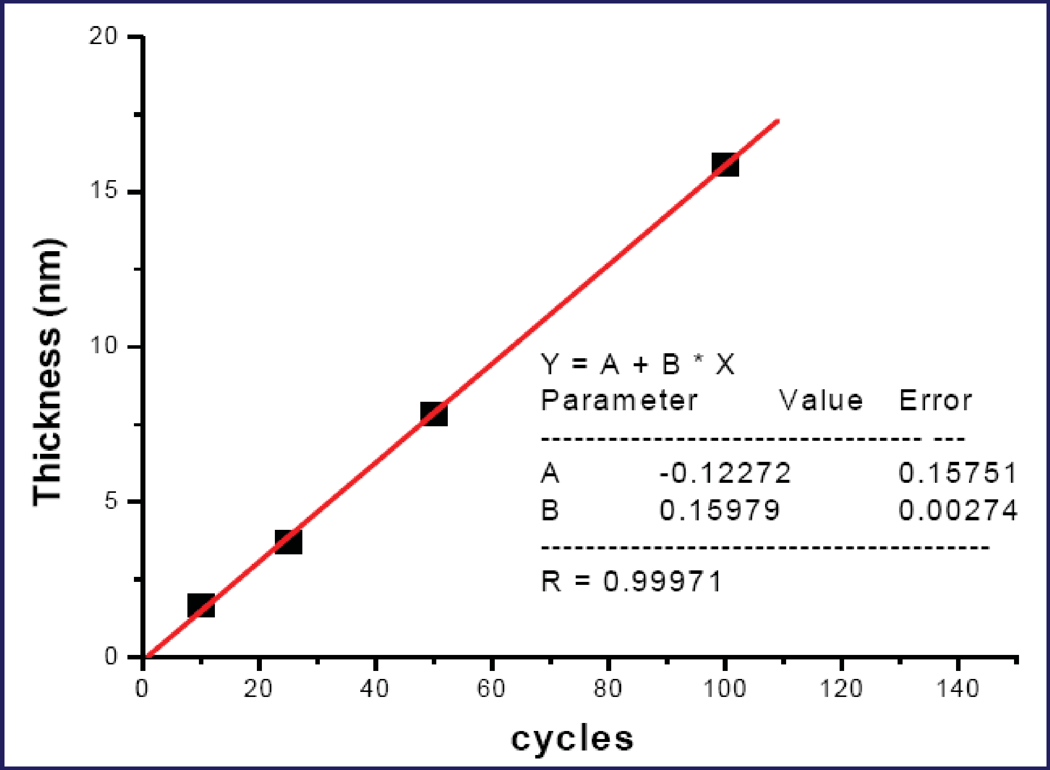
Complete evaporation without decomposition or residue

# ALE of Lanthanum Oxide, $La_2O_3$

Precursors: $H_2O$ and La(fmd)$_3$

La(fmd)$_3$ at 120 °C, substrate at 300 °C





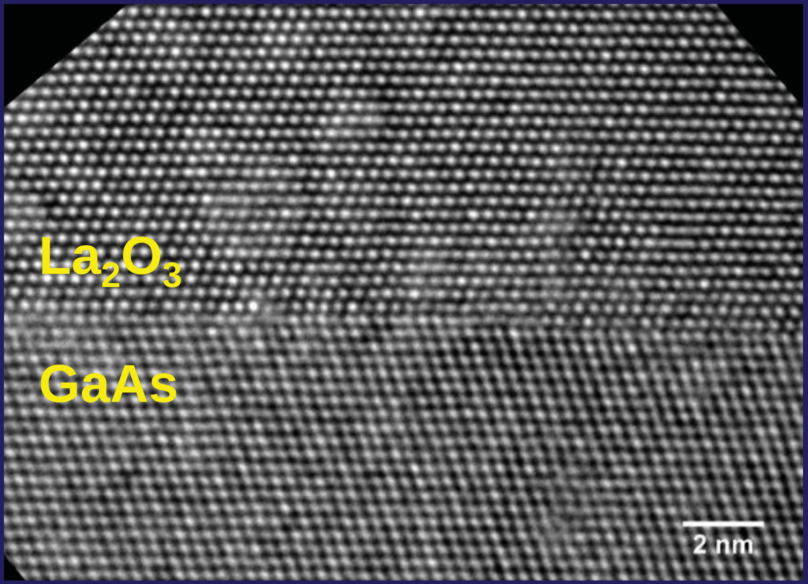
```
Y = A + B * X
Parameter       Value    Error
---------------------------------- ---
A         -0.12272        0.15751
B          0.15979        0.00274
-----------------------------------------
R = 0.99971
```

slope => 0.16 nm per cycle

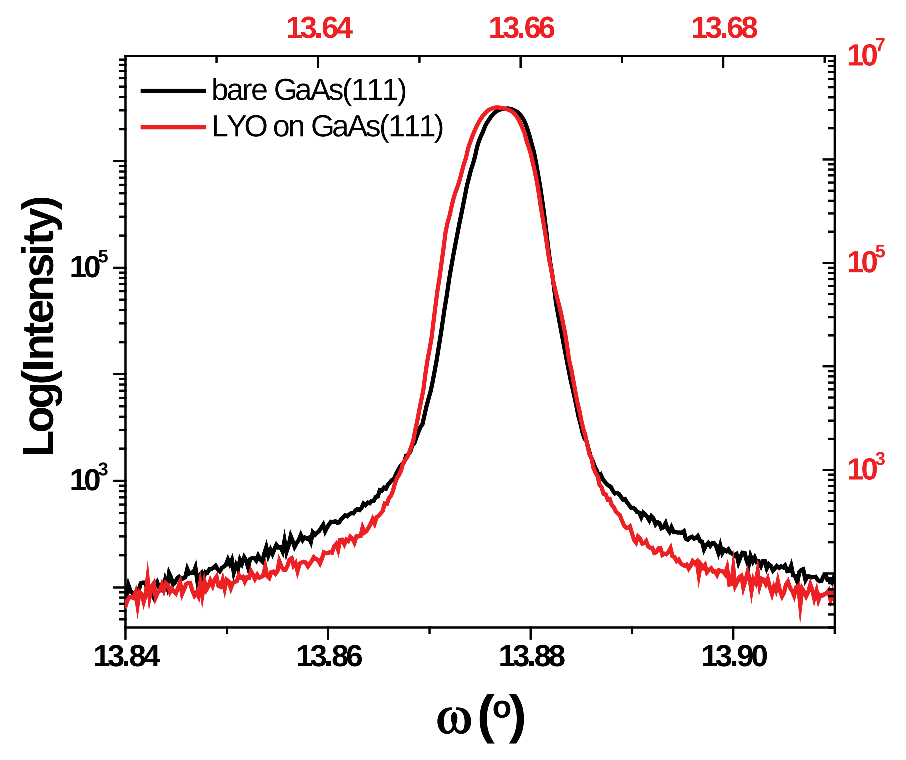
line starts at origin
=> no delay in nucleation

# ALE $La_2O_3$ is Epitaxial on GaAs(111)A

TEM



High Resolution XRD

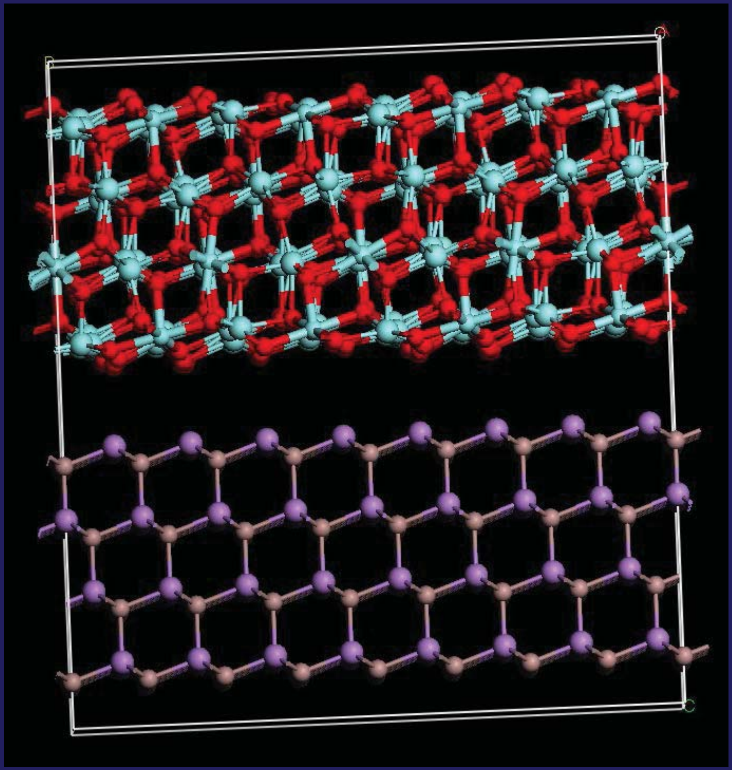


Lattice Constant Matching:

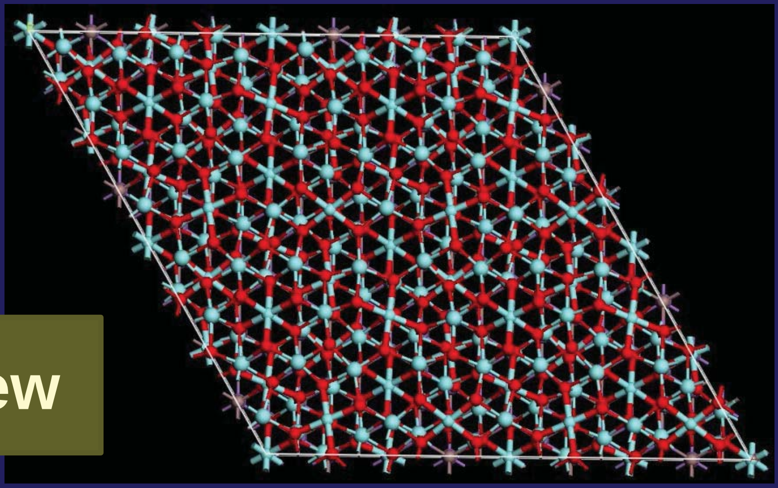
$a(La_2O_3) = 2.0008 \times a(GaAs)$

or 0.04% mismatch

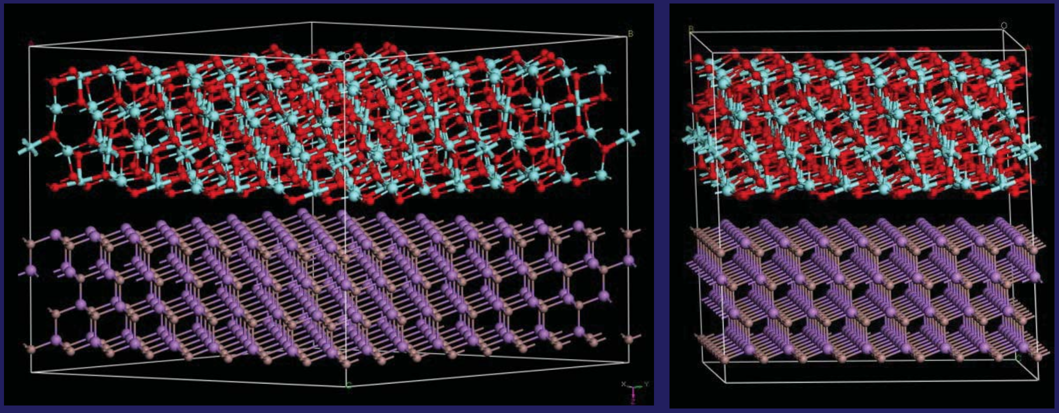
# Atomic layer epitaxy of GaAs(111)/$La_2O_3$



**Side view of GaAs(111)A/$La_2O_3$**



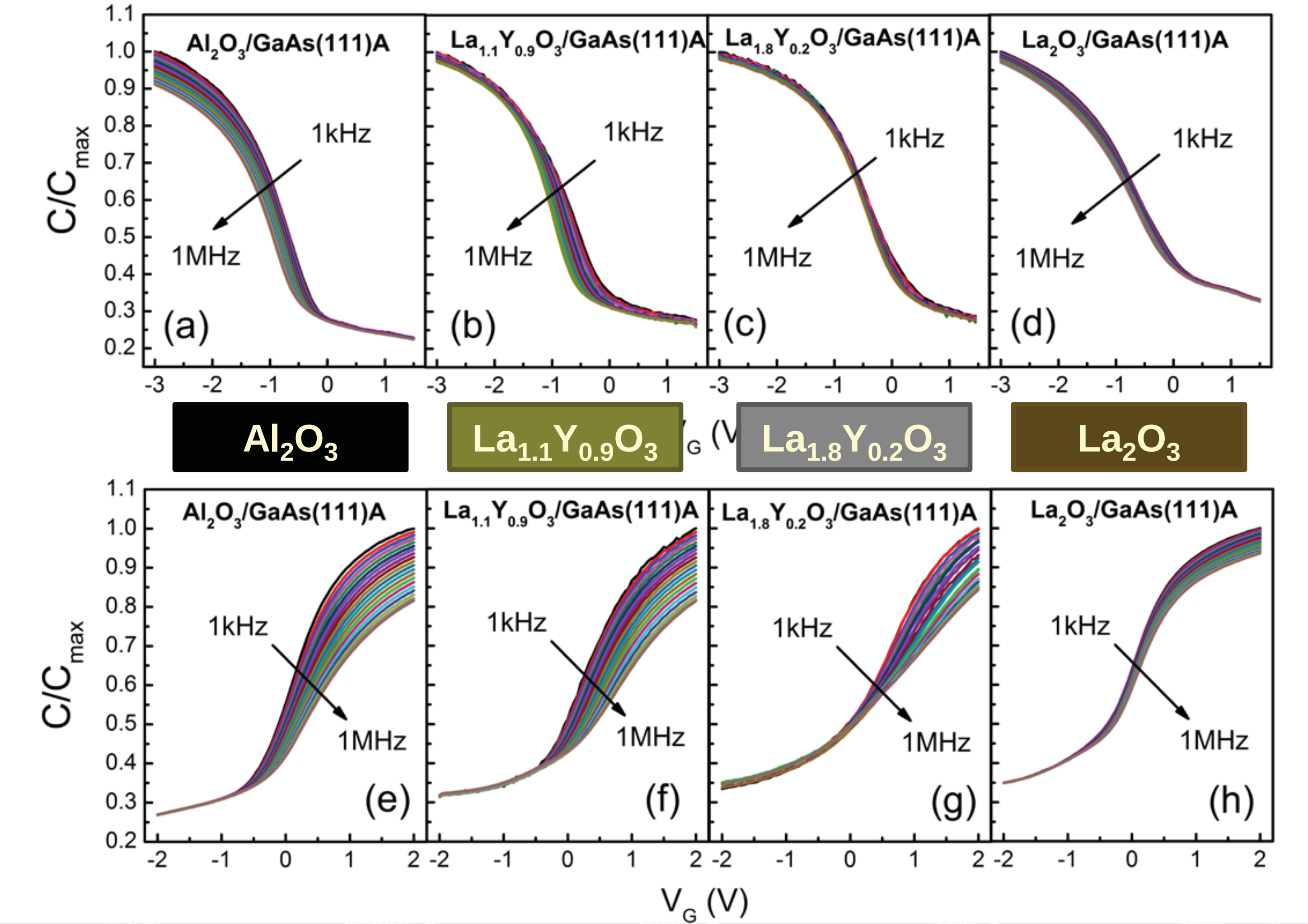
**top view**



# CV characteristics of GaAs(111)/$La_{2-x}Y_xO_3$

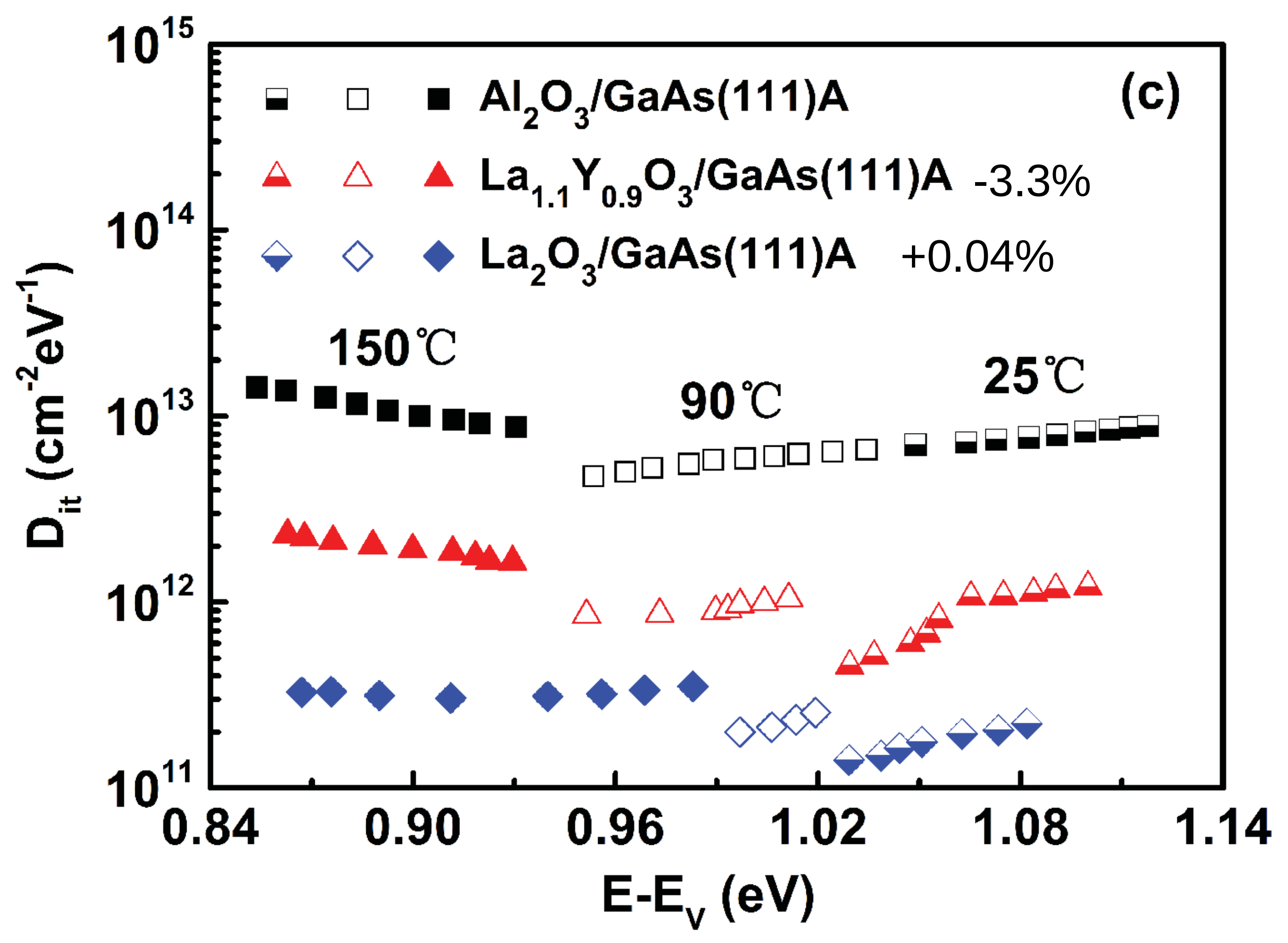
## Closer Lattice Match to GaAs => less dispersion

Mismatch => **-3.32 %** **-0.64 %** **+0.04 %**

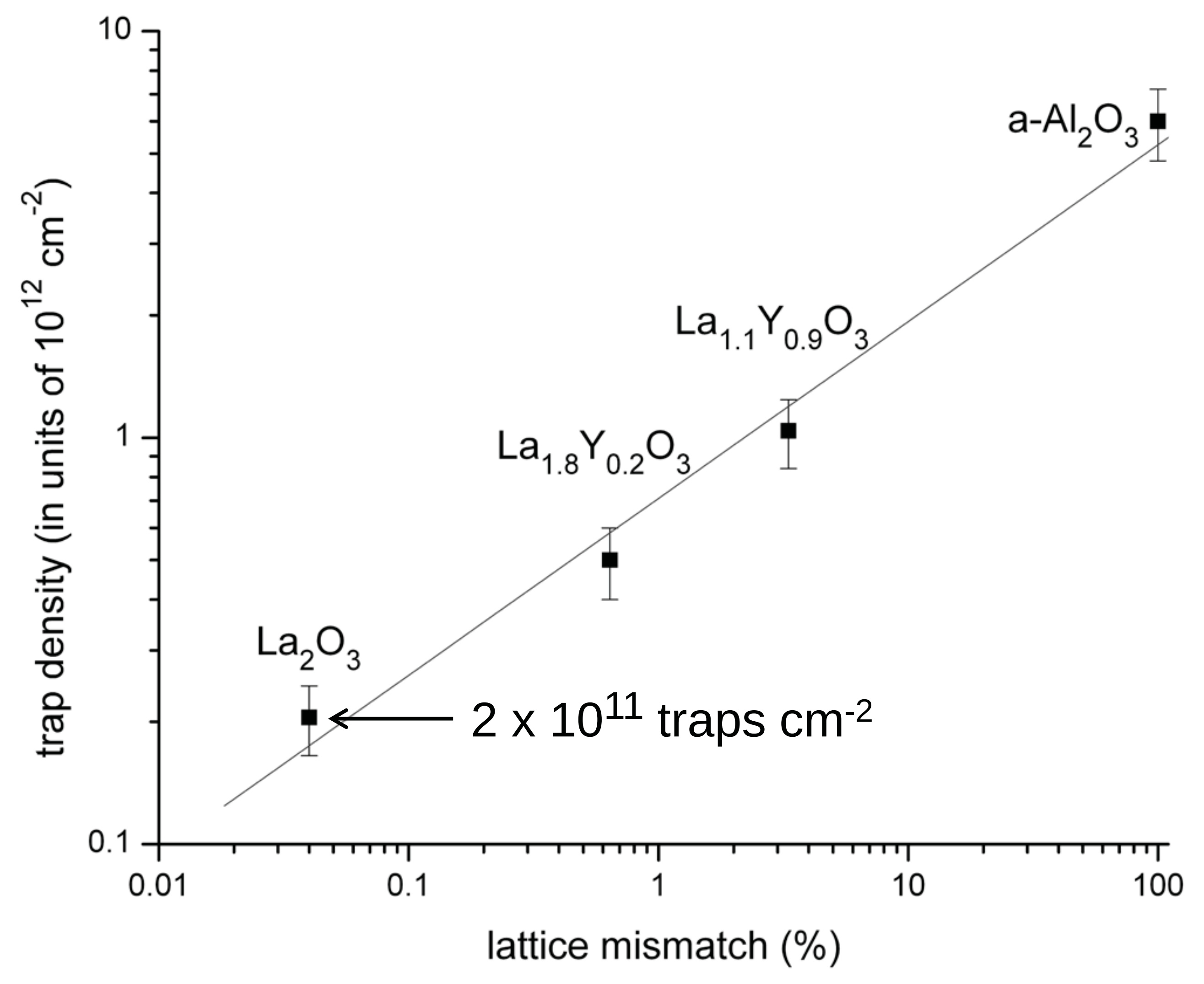


**$Al_2O_3$** **$La_{1.1}Y_{0.9}O_3$** **$La_{1.8}Y_{0.2}O_3$** **$La_2O_3$**

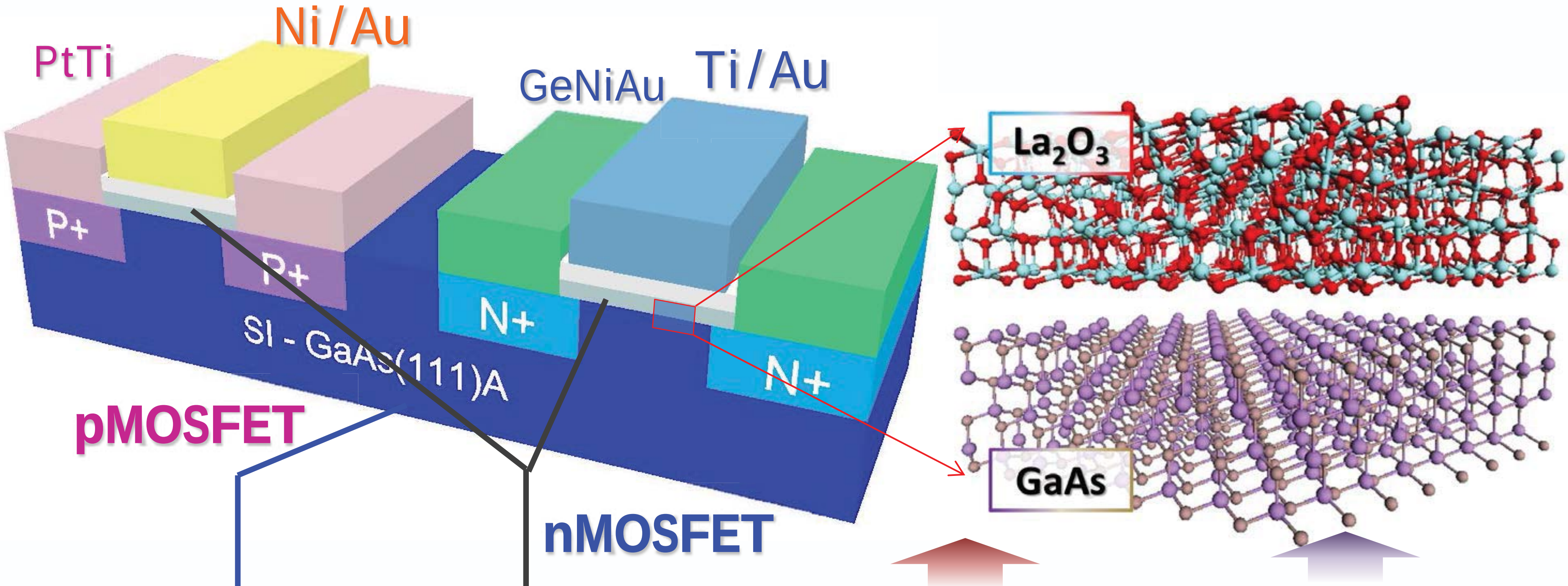
# Interface Trap Densities



# Closer Lattice Match to GaAs => Fewer Traps



# Summary of GaAs CMOS



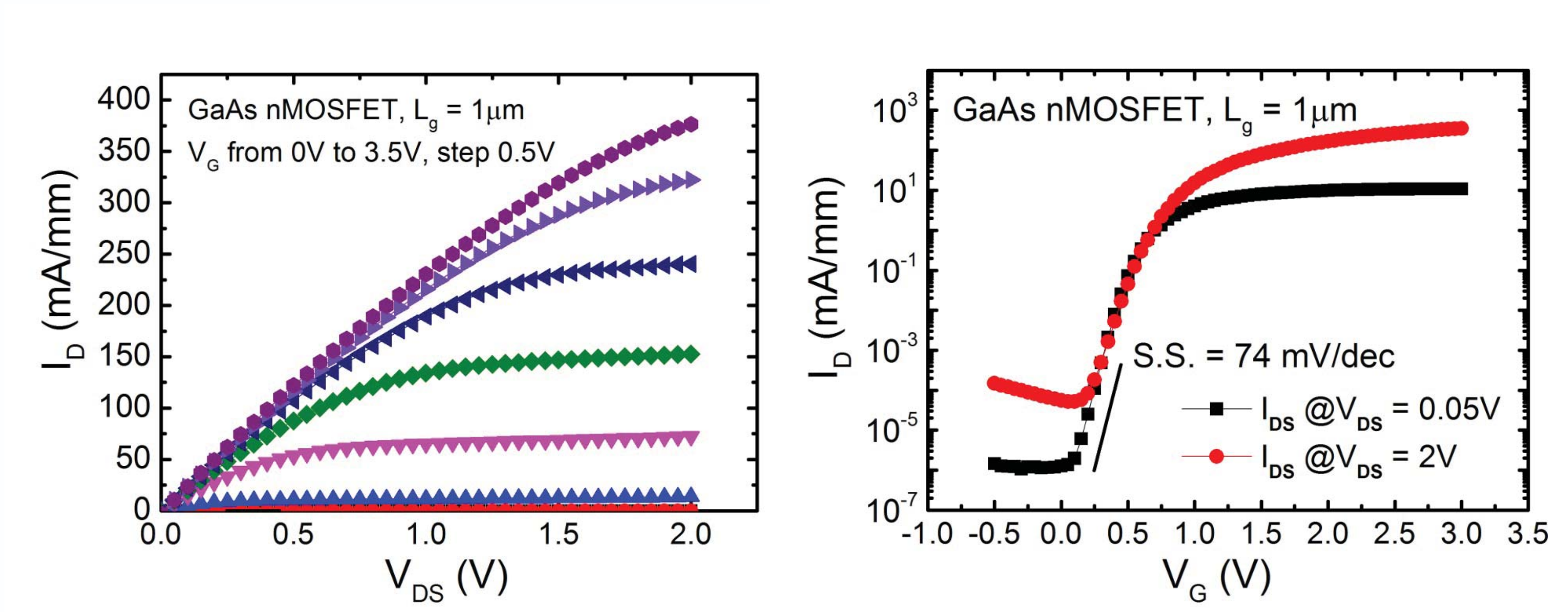
**Common substrate**

**Common dielectric**

**ALE integration**

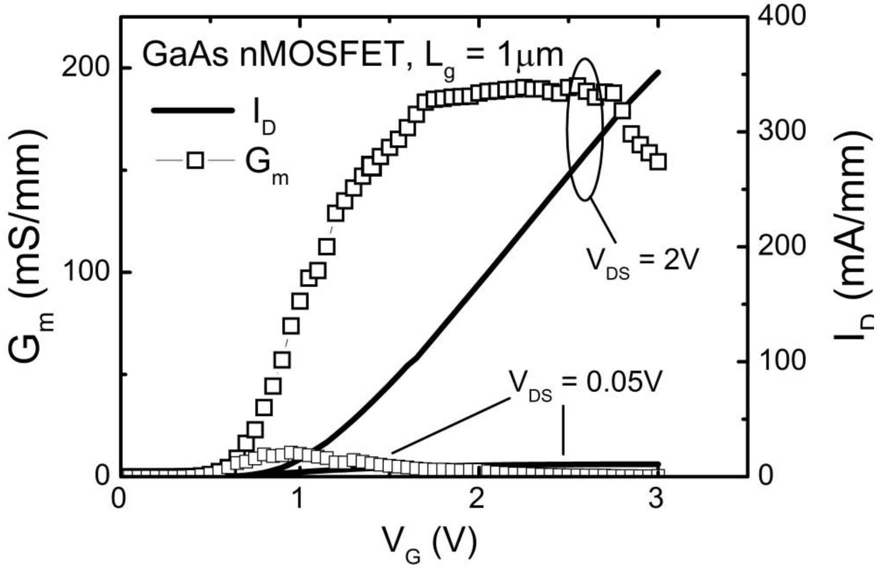
**High quality interface**

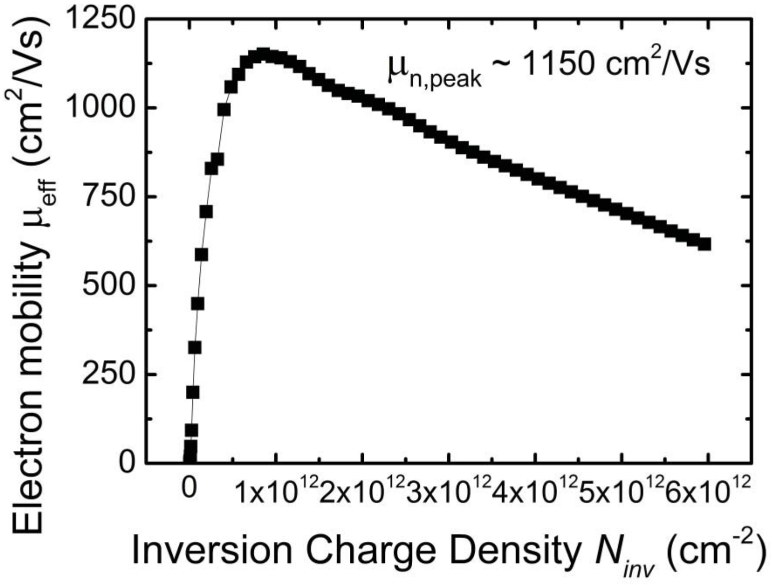
# GaAs nMOSFET with $La_2O_3$ epitaxial dielectrics



- ❑ **High drain current of 376 mA/mm is obtained from GaAs nMOSFET with 1μm gate length**
- ❑ **Current $I_{on}/I_{off}$ ~$10^7$, subthreshold slope as low as 74 mV/dec**
- ❑ **A mean $D_{it}$ of $1.7\times10^{12}$ $cm^{-2}\cdot eV^{-1}$, using $SS = 60(1+qD_{it}/C_{ox})$**

# GaAs nMOSFET with $La_2O_3$ epitaxial dielectric

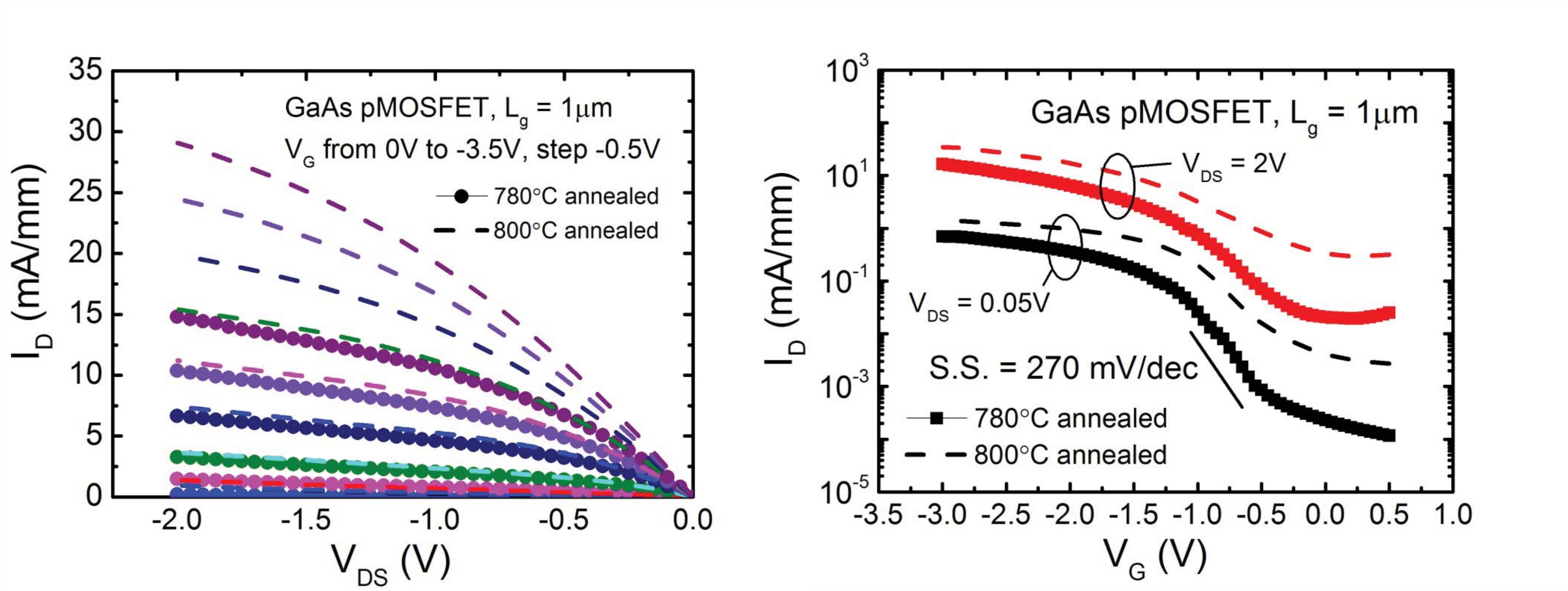




❑ **Peak transconductance $G_m$ ~190 mS/mm**

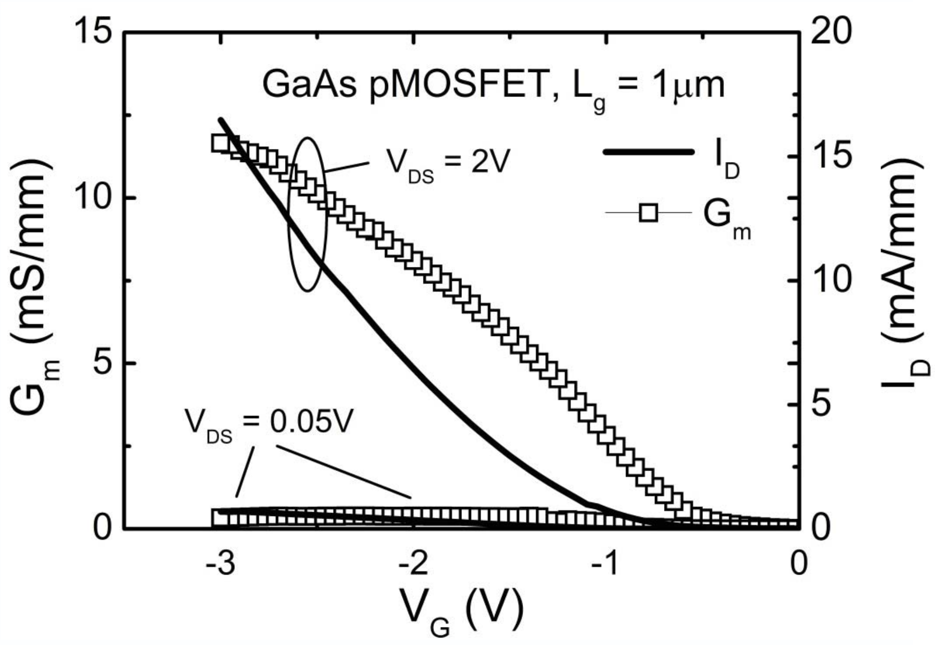
❑ **Peak electron effective mobility ~1150 $cm^2/Vs$**

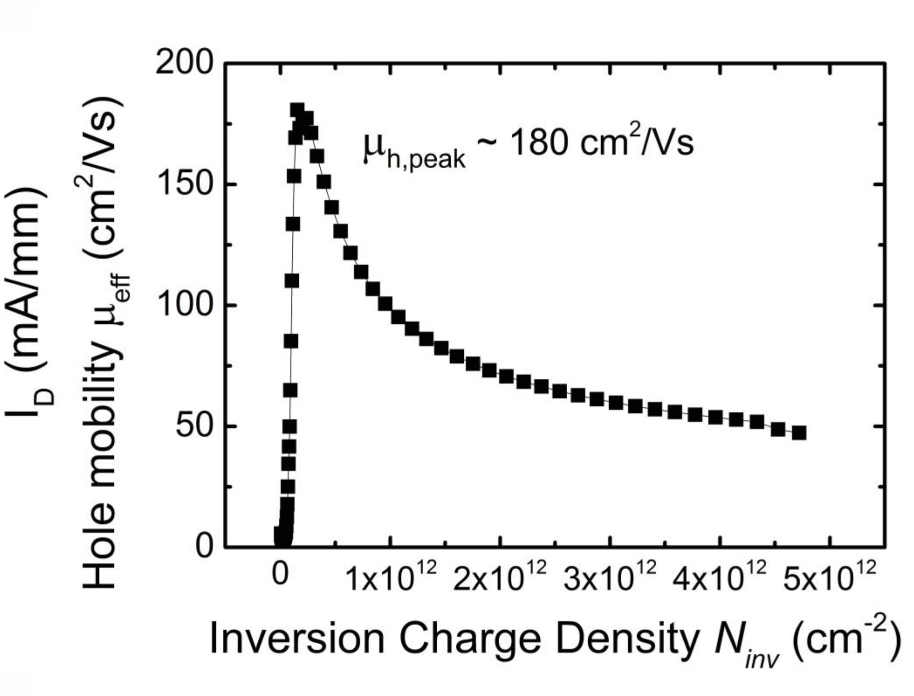
# GaAs pMOSFET with $La_2O_3$ epitaxial dielectric



- **Maximum drain current of 30 mA/mm is obtained from GaAs pMOSFET with 1μm gate length**
- **$I_{on}/I_{off}$ ~$10^4$ and ~$10^3$ for the pMOSFETs with 1μm gate** length annealed at 780˚C and 800˚C, respectively

# GaAs pMOSFET with $La_2O_3$ epitaxial dielectric

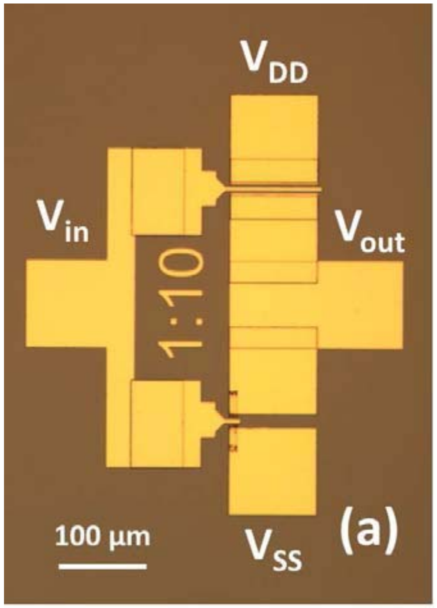


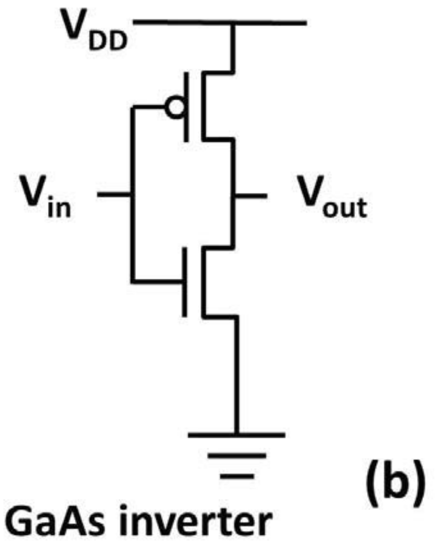


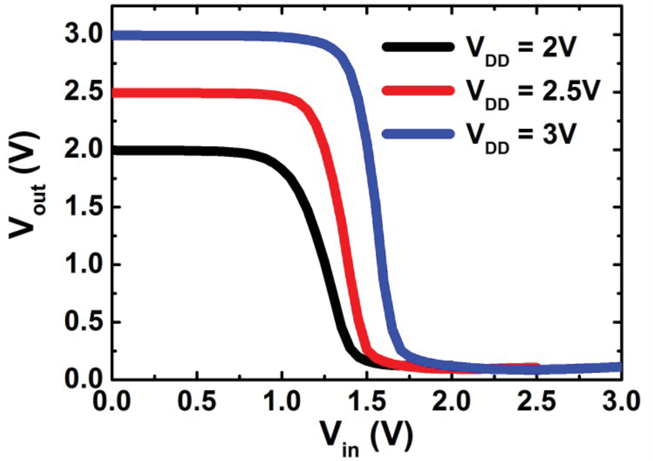
- ❑ A transconductance of 12 mS/mm is obtained from GaAs pMOSFET with Lg = 1µm

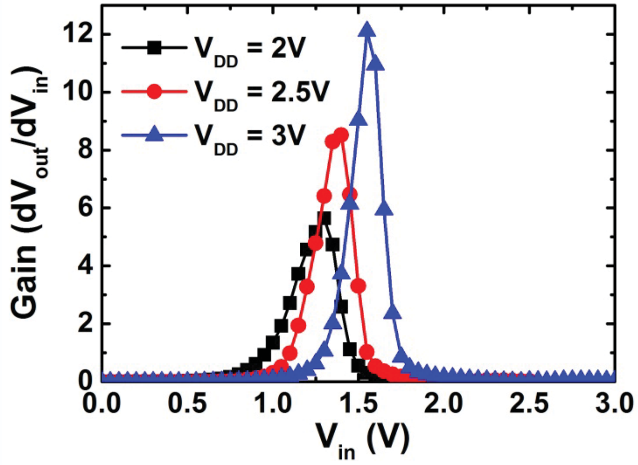
- ❑ The peak effective hole mobility is around 180 $cm^2/Vs$.

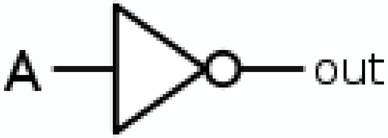
# CMOS GaAs inverters





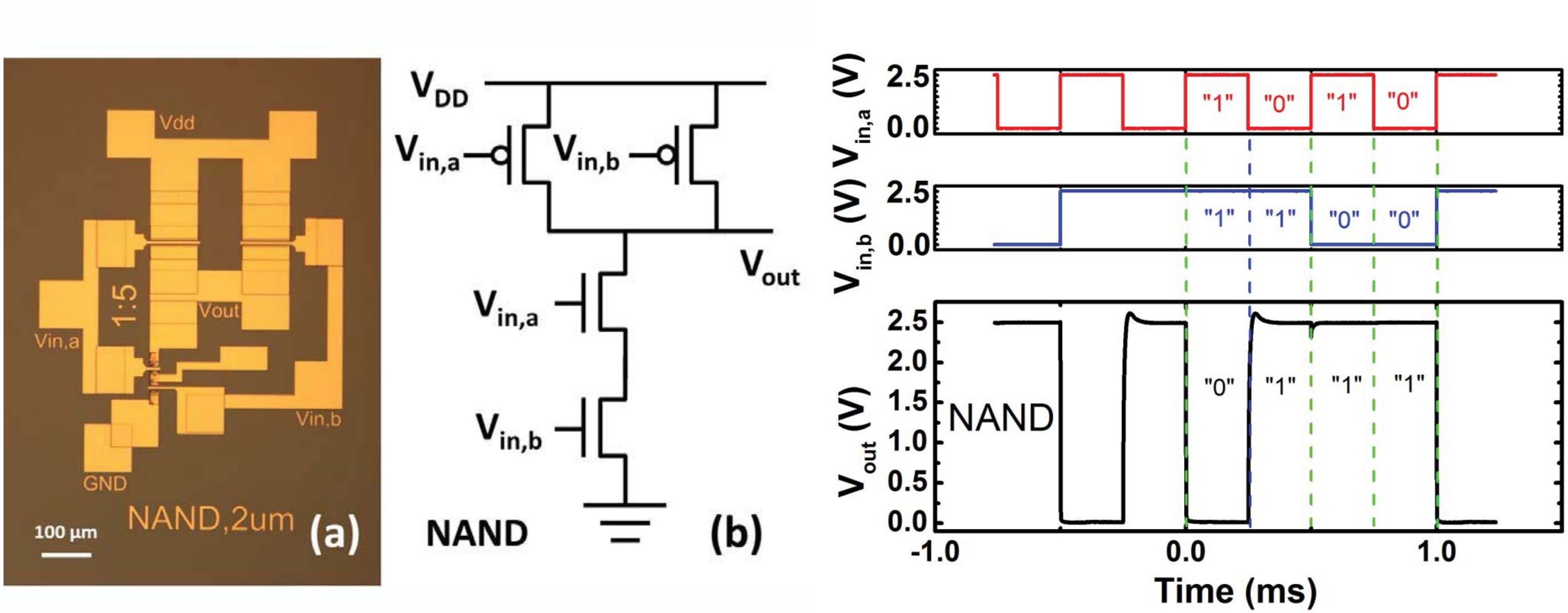


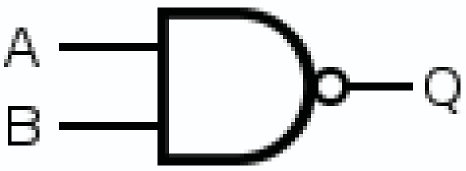




- ☐ **Peak gain of 12 is obtained with $V_{DD}$ = 3V**

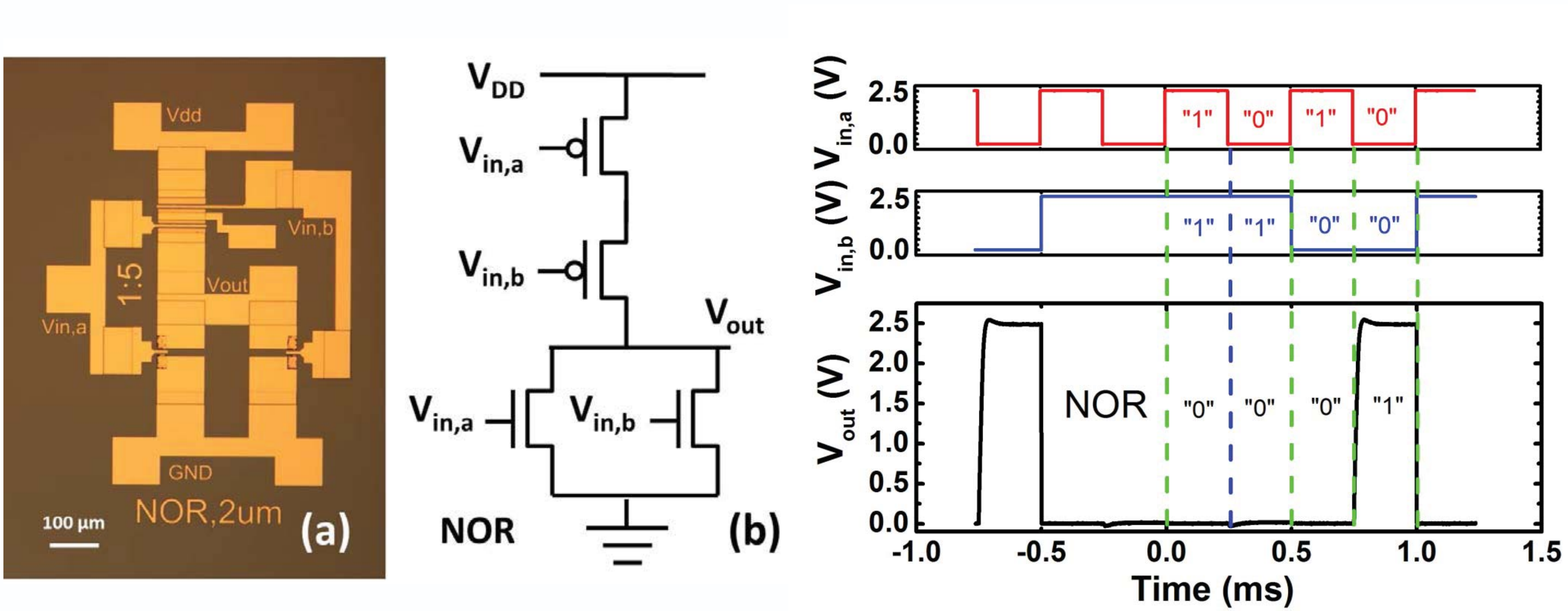
# CMOS GaAs NAND logic gate

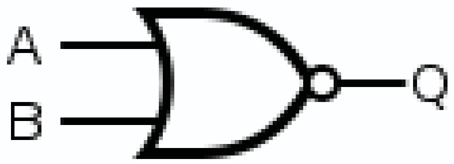




| | | | | | | |
|---|---|---|---|---|---|---|
| NAND logic | Inputs | $V_{in,a}$ | 1 | 0 | 1 | 0 |
| | | $V_{in,b}$ | 1 | 1 | 0 | 0 |
| | Output | $V_{out}$ | 0 | 1 | 1 | 1 |

# CMOS GaAs NOR logic gate

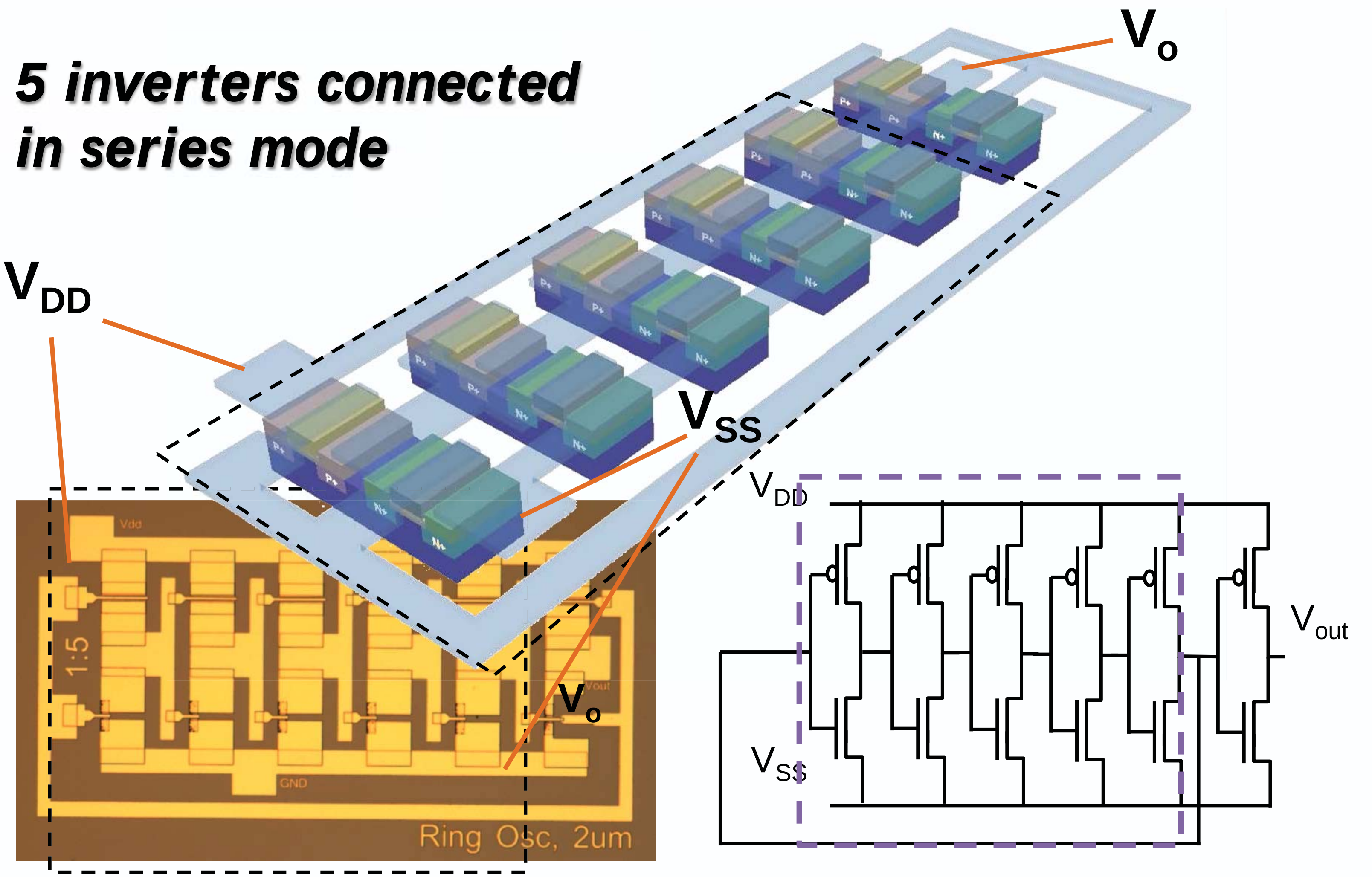




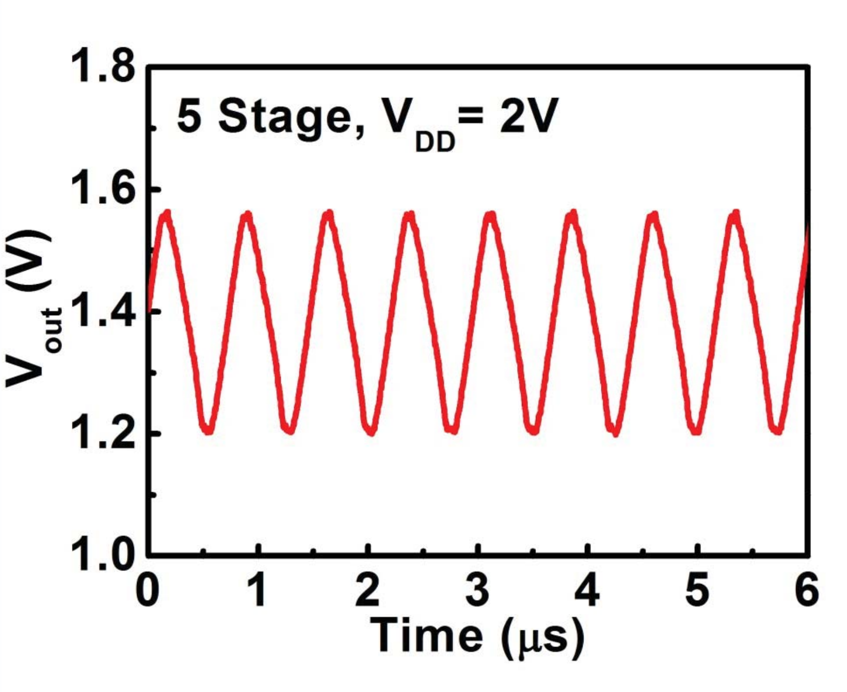
| | | | | | | |
|---|---|---|---|---|---|---|
| NOR logic | Inputs | $V_{in,a}$ | 1 | 0 | 1 | 0 |
| | | $V_{in,b}$ | 1 | 1 | 0 | 0 |
| | Output | $V_{out}$ | 0 | 0 | 0 | 1 |

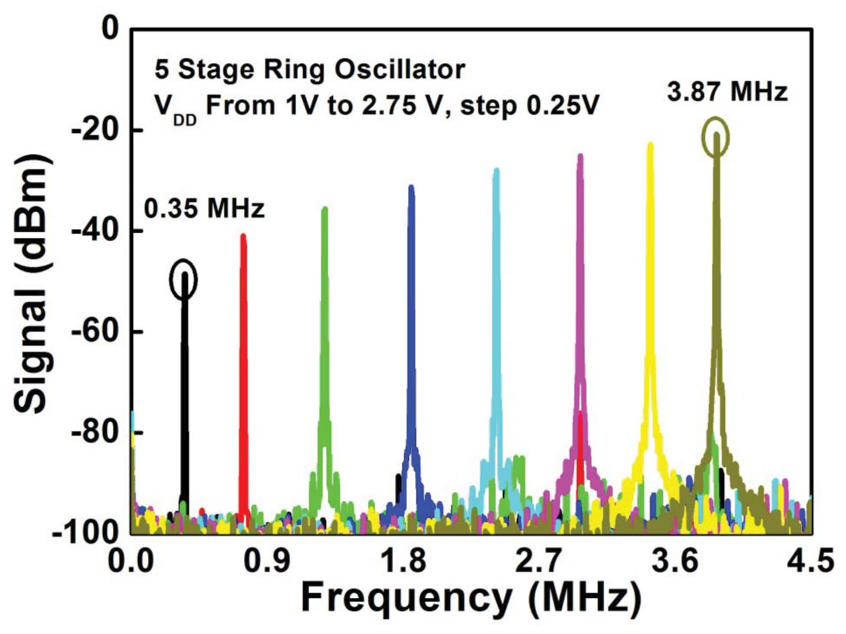
# CMOS GaAs 5-stage ring oscillator

***5 inverters connected in series mode***



# CMOS GaAs 5-stage ring oscillator



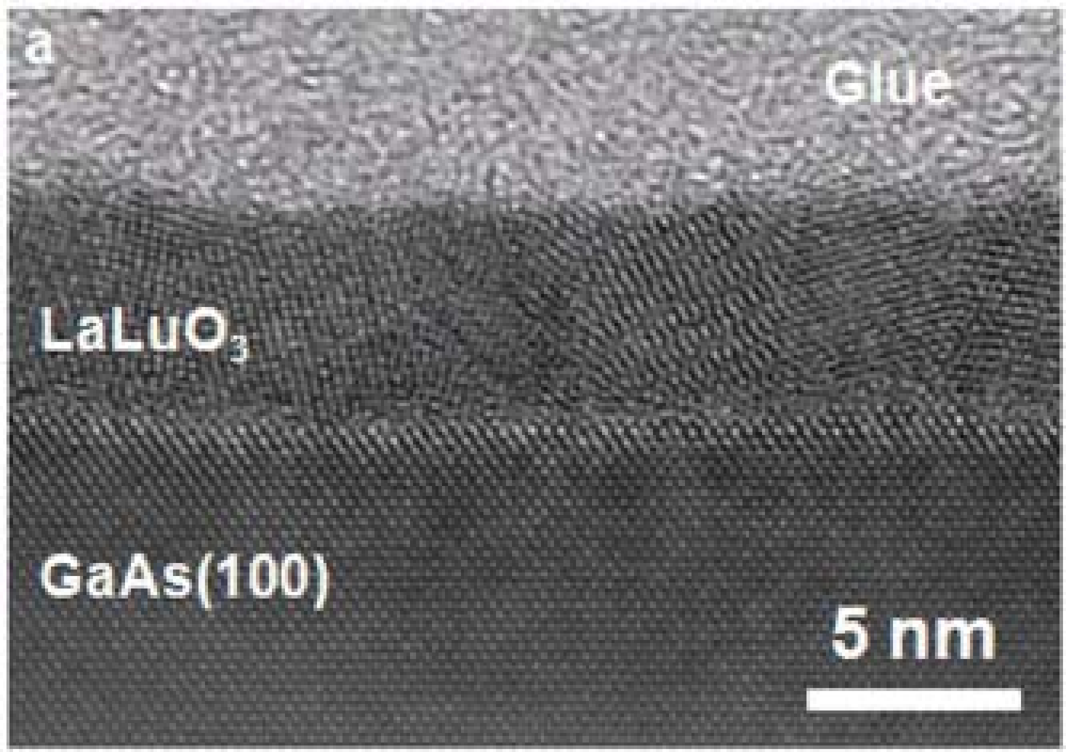


- At $V_{DD}$ =2 V, the fundamental oscillation frequency is at 2.2 MHz
- The fundamental resonance frequency increases from 0.35 MHz at $V_{DD}$=1 V to 3.87 MHz at $V_{DD}$=2.75 V.

**Acknowledgement: Y.Q. Wu/HUST**

# How to Translate these Results to GaAs(100)

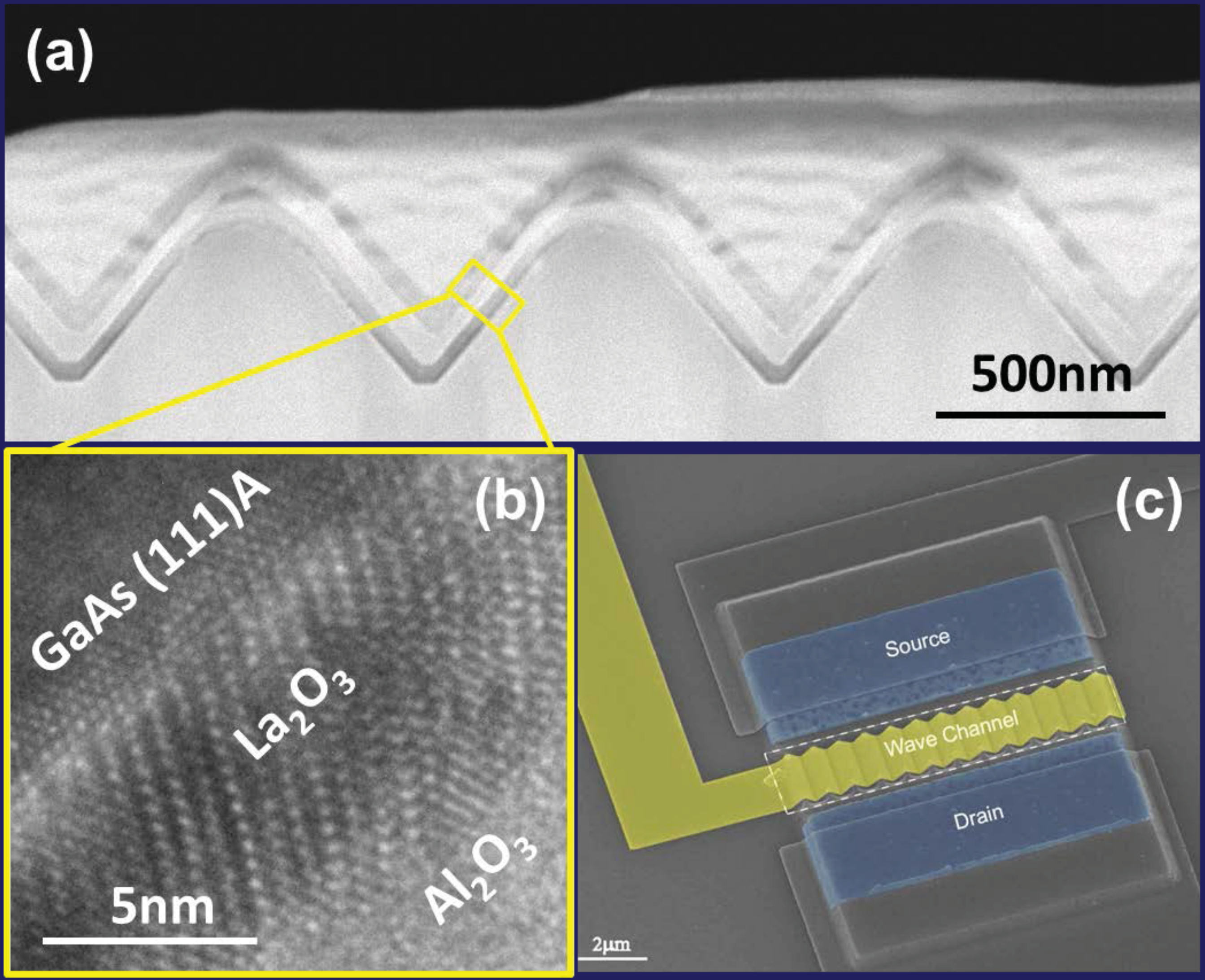
ALE $La_2O_3$ and $LaLuO_3$ are polycrystalline, not epitaxial, on GaAs(100)



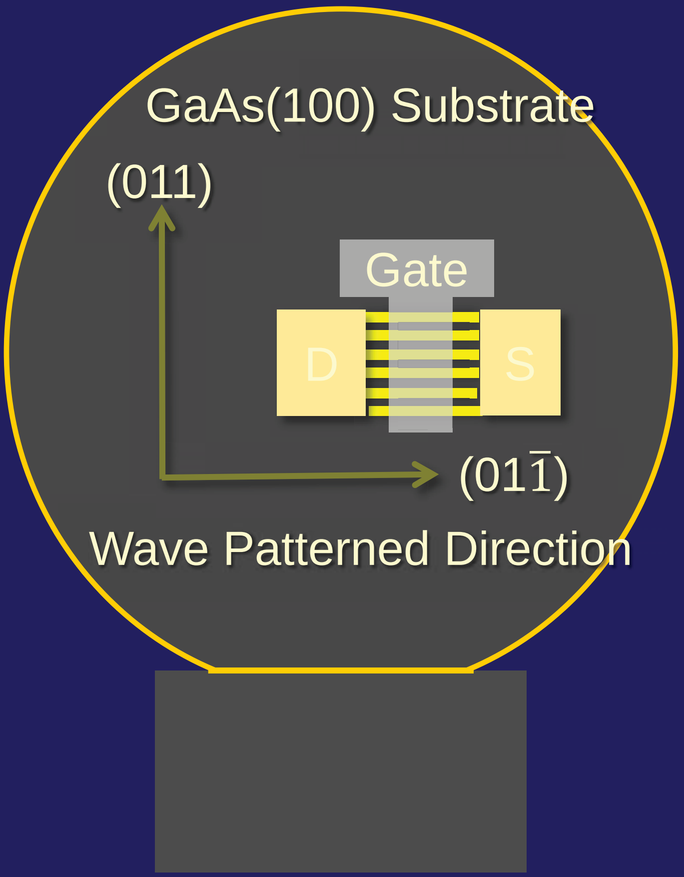
Electrical measurements of capacitors show many traps at interface

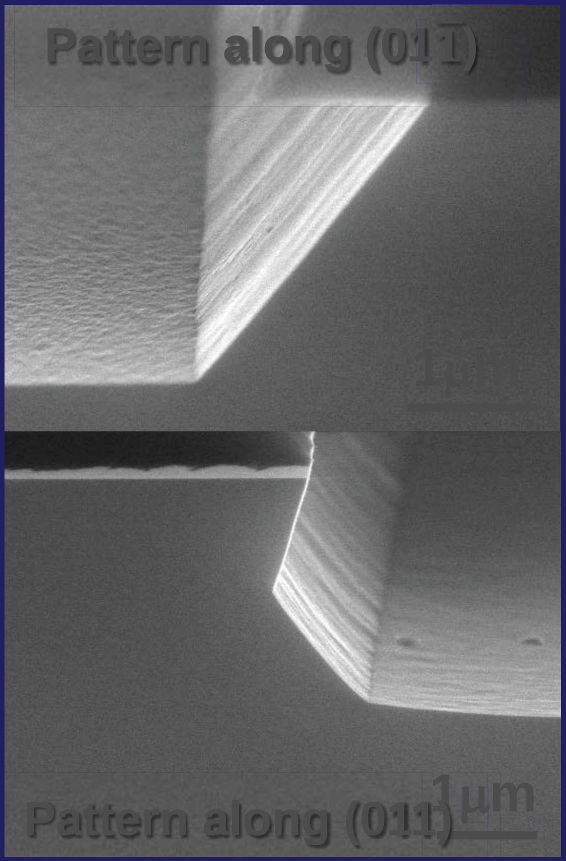
# Wet Etching GaAs(100) Exposes (111) Surface

=> epitaxial $La_2O_3$ on GaAs(111) facets

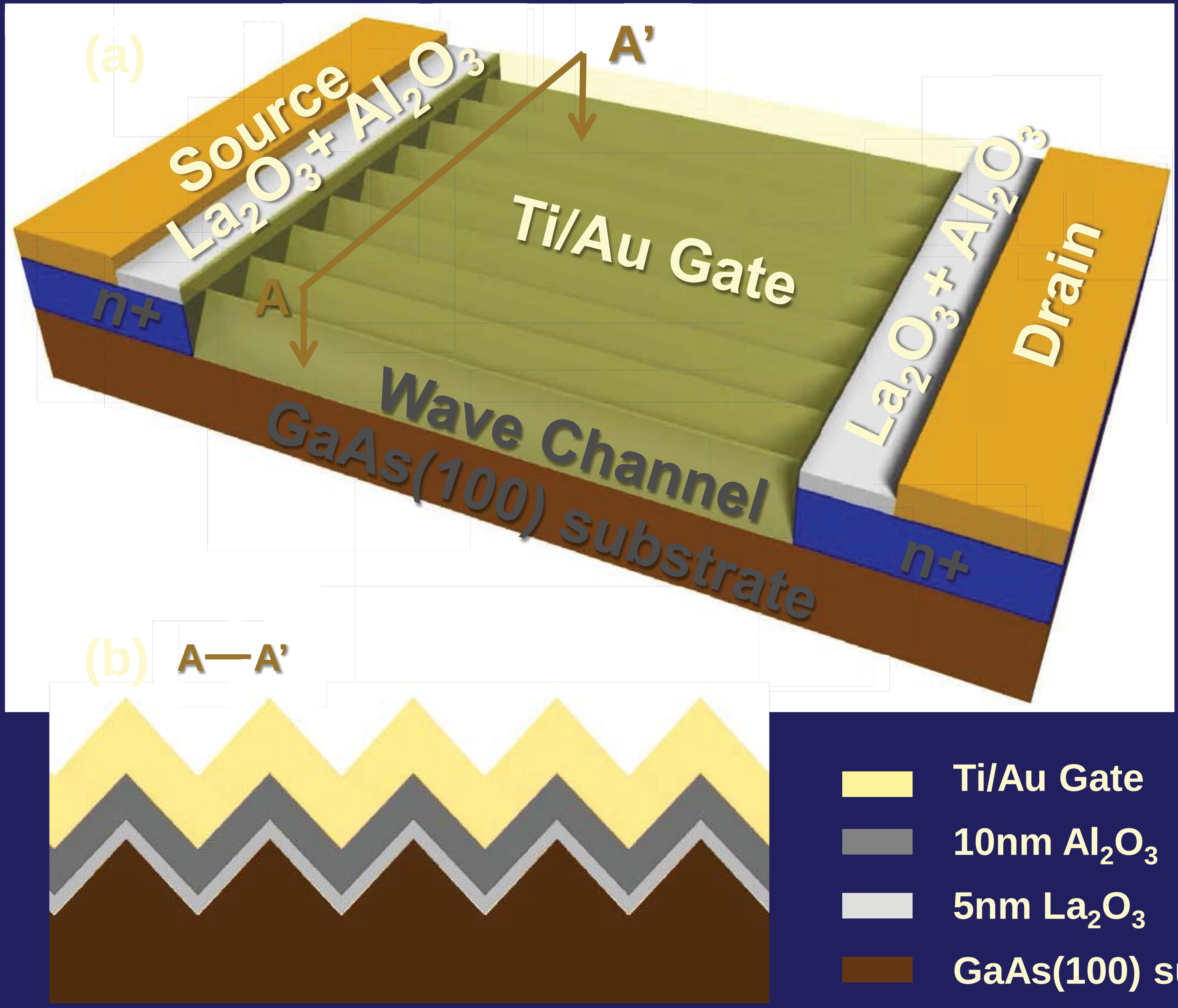


# Orientation to Form GaAs(111) Facets



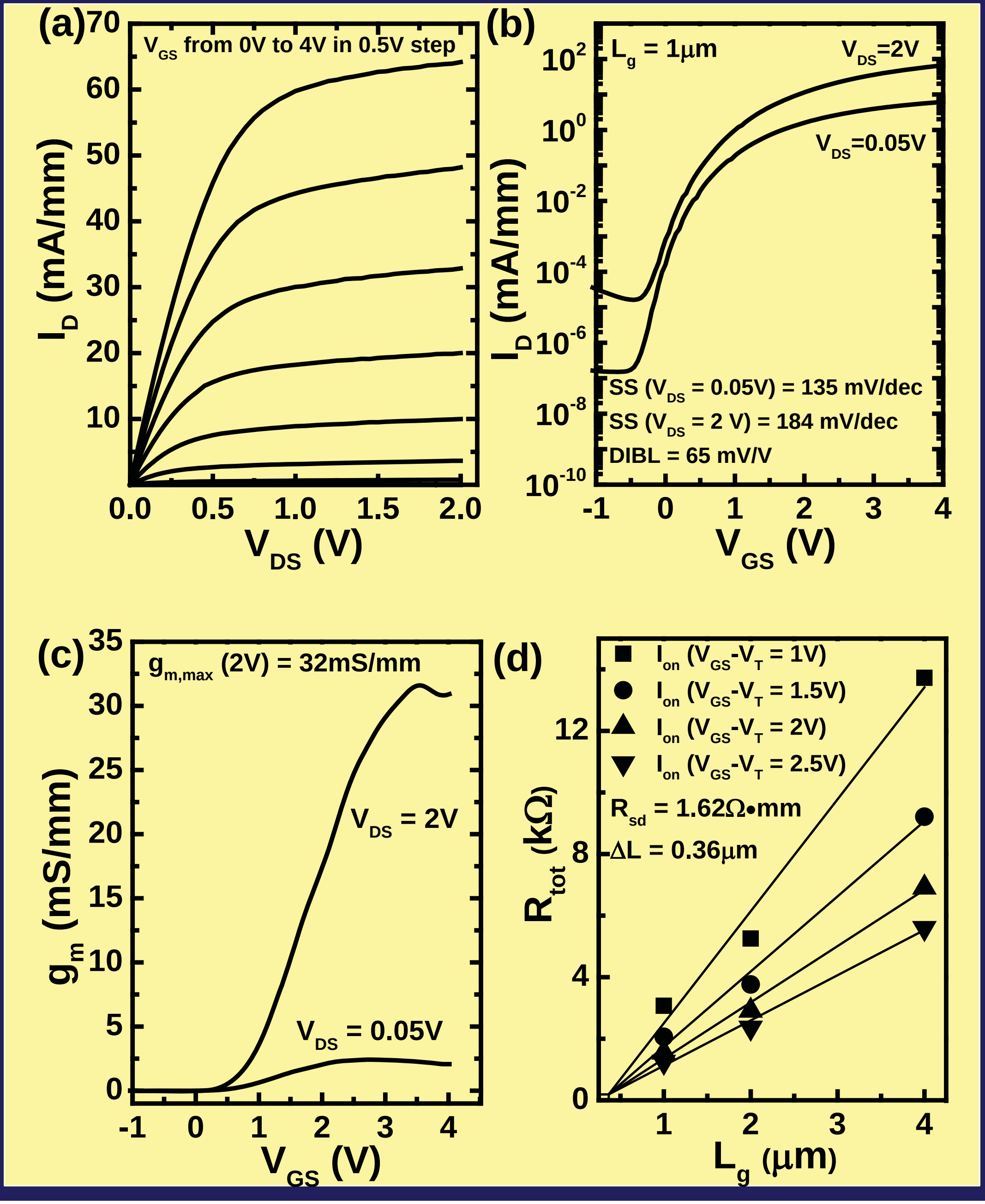


# WaveFET Structure on GaAs(100)

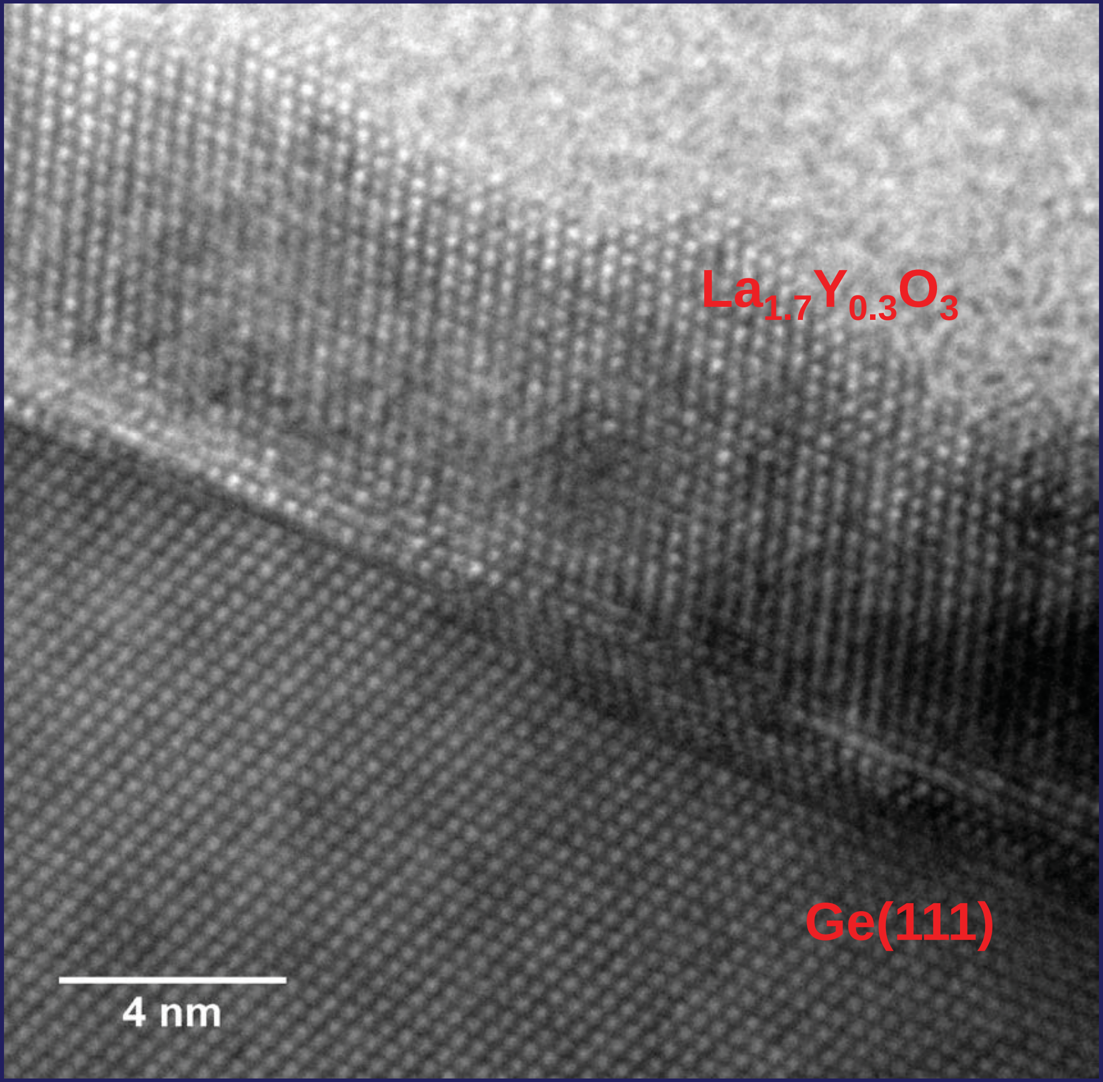


- 🟨 Ti/Au Gate
- ▨ 10nm $Al_2O_3$
- ☐ 5nm $La_2O_3$
- 🟫 GaAs(100) substrate

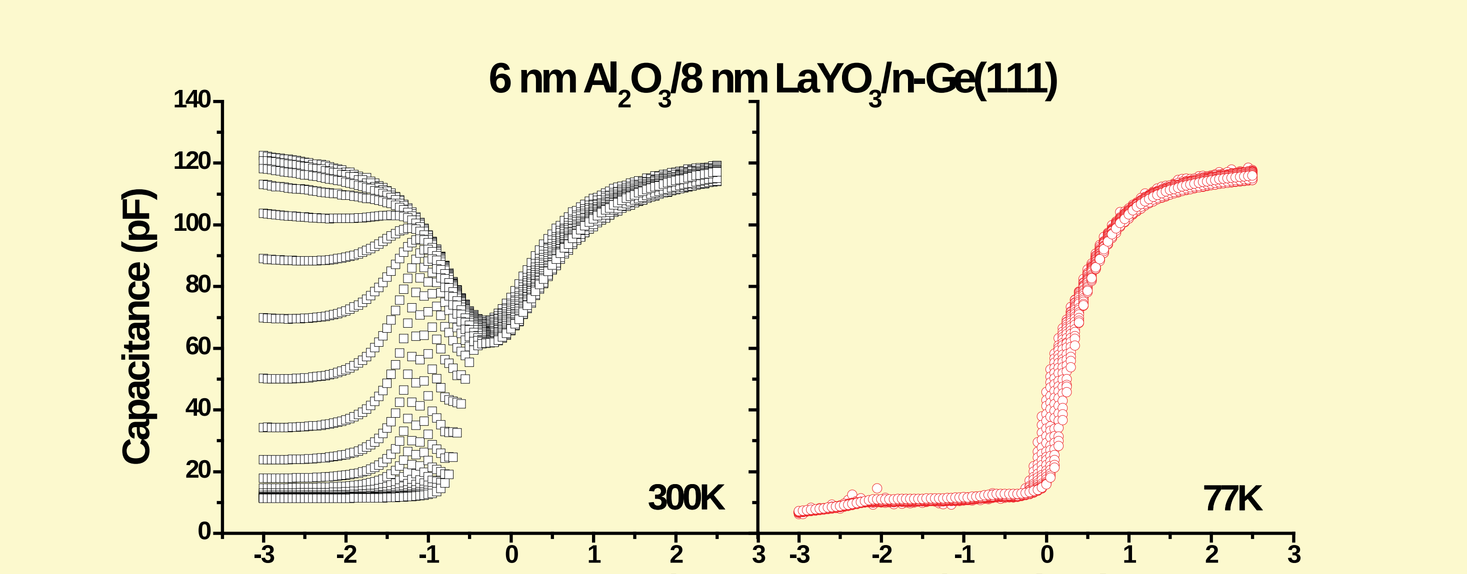
# WaveFET GaAs Transistor Performance



# Epitaxy of $La_{1.7}Y_{0.3}O_3$ on Ge(111)

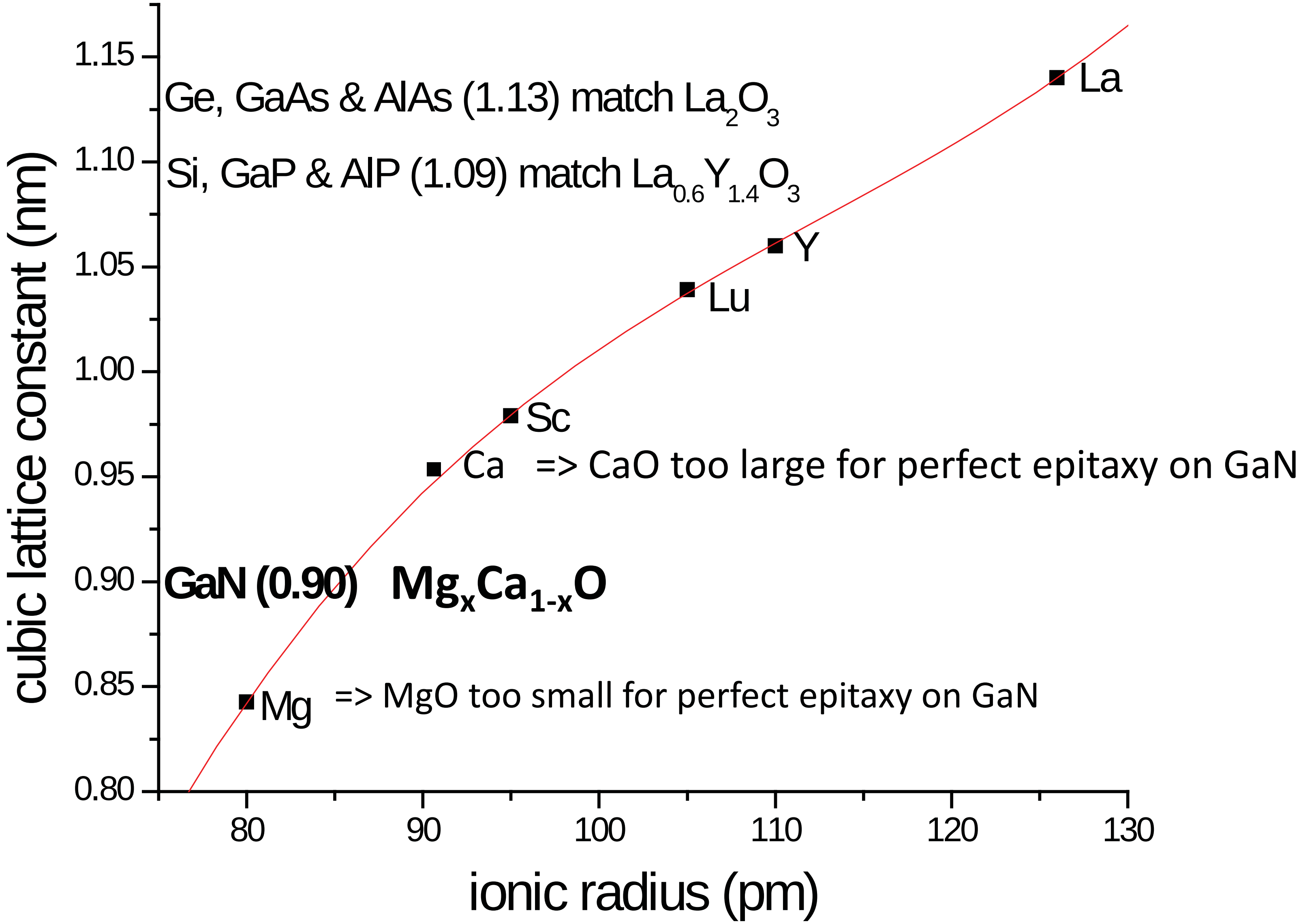


# Capacitors with (La,Y)$_2$O$_3$ on Ge(111)



High-performance pMOS transistors are expected using this epitaxial interface

# Possible Epitaxial Oxides for GaN



Ge, GaAs & AlAs (1.13) match $La_2O_3$

Si, GaP & AlP (1.09) match $La_{0.6}Y_{1.4}O_3$

Ca => CaO too large for perfect epitaxy on GaN

**GaN (0.90)** **$Mg_xCa_{1-x}O$**

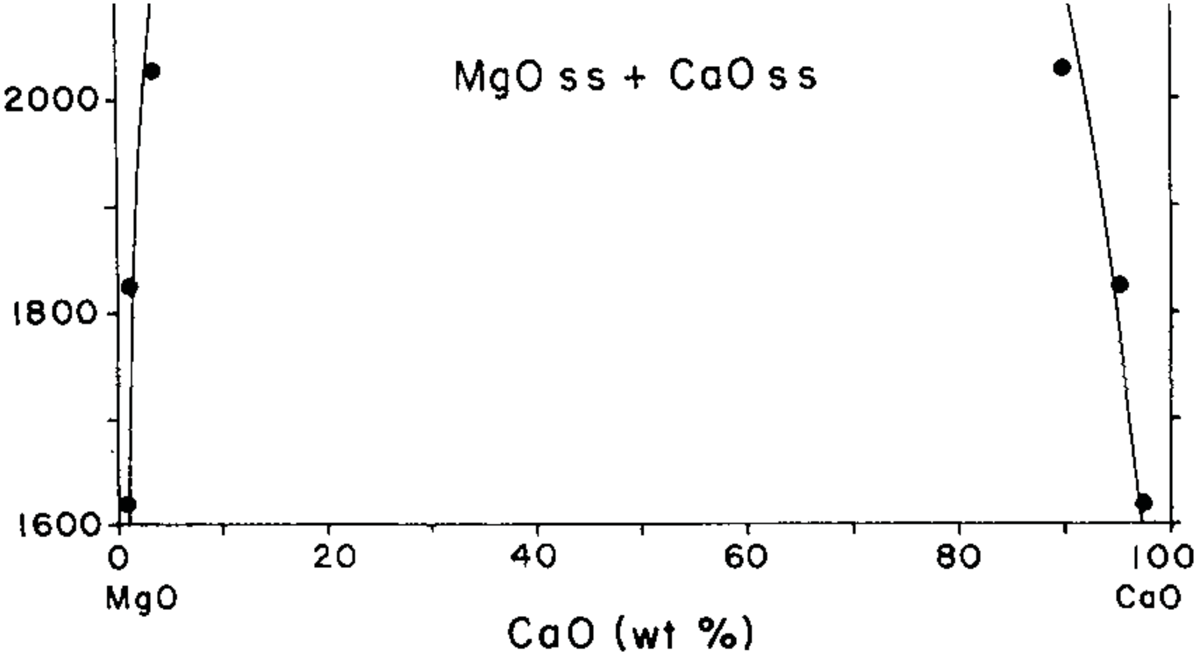
Mg => MgO too small for perfect epitaxy on GaN

# Phase Diagram of (Ca,Mg)O

Miscibility gap for
most compositions

Metastable compositions
decompose at about 600 $^{o}$C

=> Need to deposit
(Ca,Mg)O at T < 600 $^{o}$C
to avoid decomposition

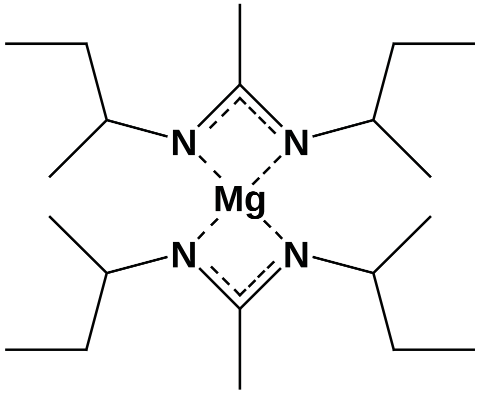


**Phase equilibrium diagram for the system CaO–MgO. Solid**

J. Am. Ceram. Soc. **46,** 314 (1963)

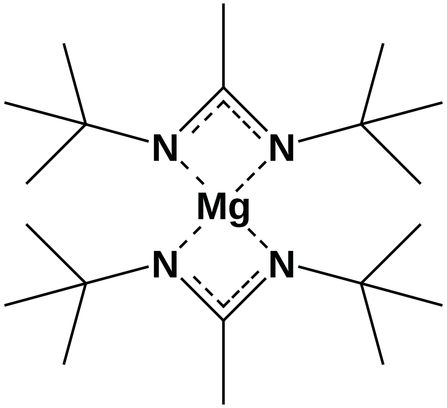
# 2 Precursors for ALE of Magnesium Oxide, MgO

**bis(*N,N'*-di-*sec*-butylacetamidinato) magnesium**



**Liquid**

**bis(*N,N'*-di-*tert*-butylacetamidinato) magnesium**



**Solid**

**ALD bubbler temperatures 90 – 110 $^{o}$C**

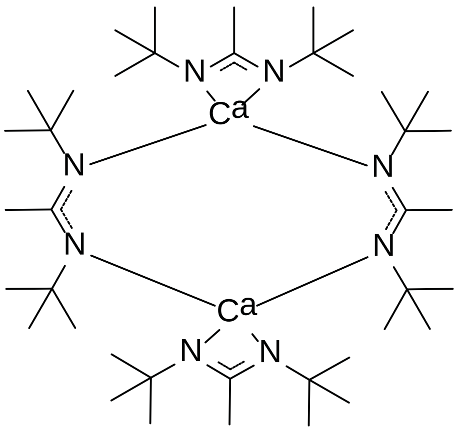
**Residue < 1% (clean evaporation)**

**Chose the liquid on left because of its ready purification by distillation and easier handling**

**ALD of MgO at 300 $^{o}$C, low enough to avoid thermal decomposition of (Ca,Mg)O**

# 3 Precursors for ALE of Calcium Oxide

**bis(*N,N’*-di-*tert*-butyl-acetamidinato) calcium**

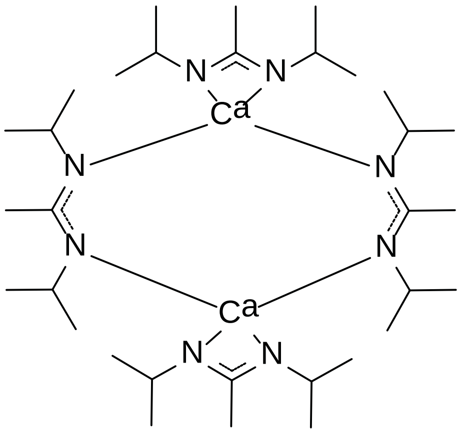


Sublimes at 185-190$^o$C

Low volatility

Reactive to $H_2O$

**bis(*N,N’*-diisopropyl-acetamidinato) calcium**

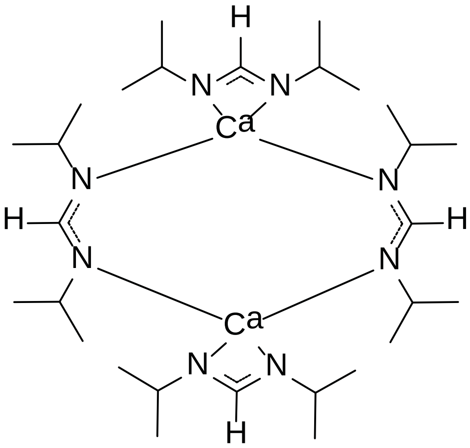


Sublimes at 135-140$^o$C

Higher volatility

Reactive to $H_2O$

**bis(*N,N’*-diisopropyl-formamidinato) calcium**



**Sublimes at 95-100$^o$C**

**Superior precursor:**

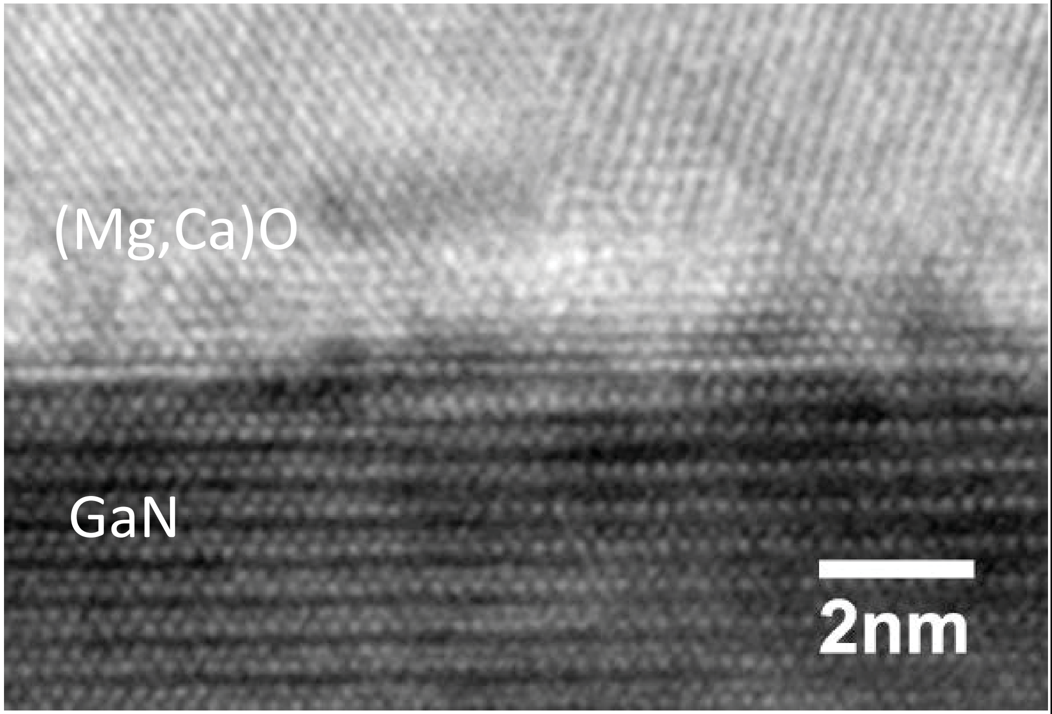
**Highest volatility**

**Reactive to $H_2O$**

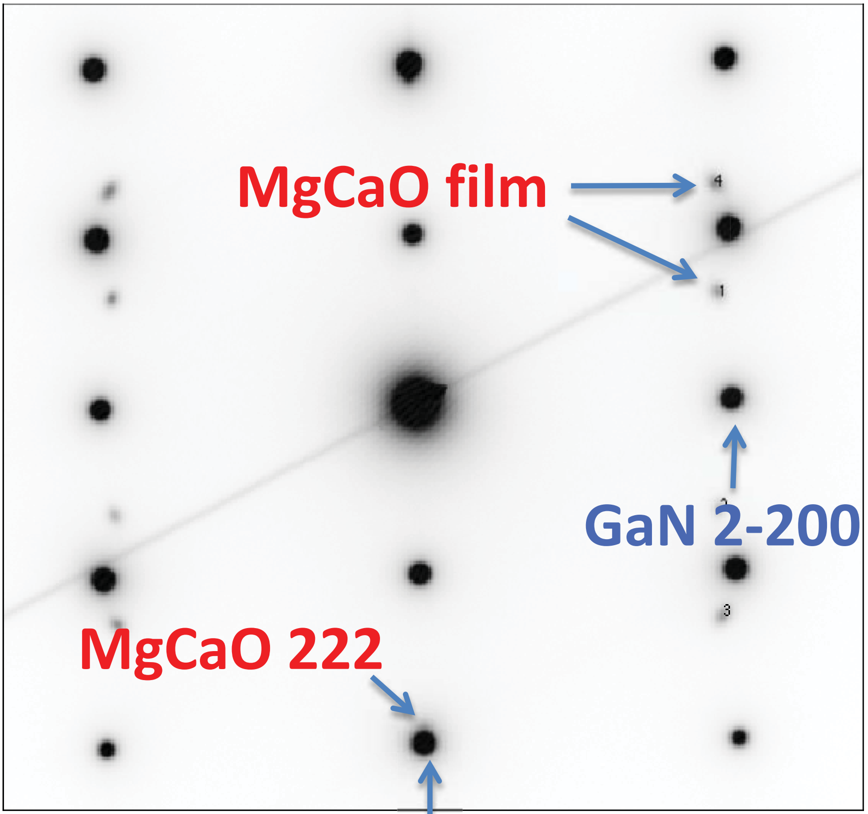
**Scaled up production**

**ALD of CaO at 300 $^o$C, low enough to avoid decomposition of (Ca,Mg)O**

# Electron Diffraction from Epitaxial (Ca,Mg)O on GaN(0001)

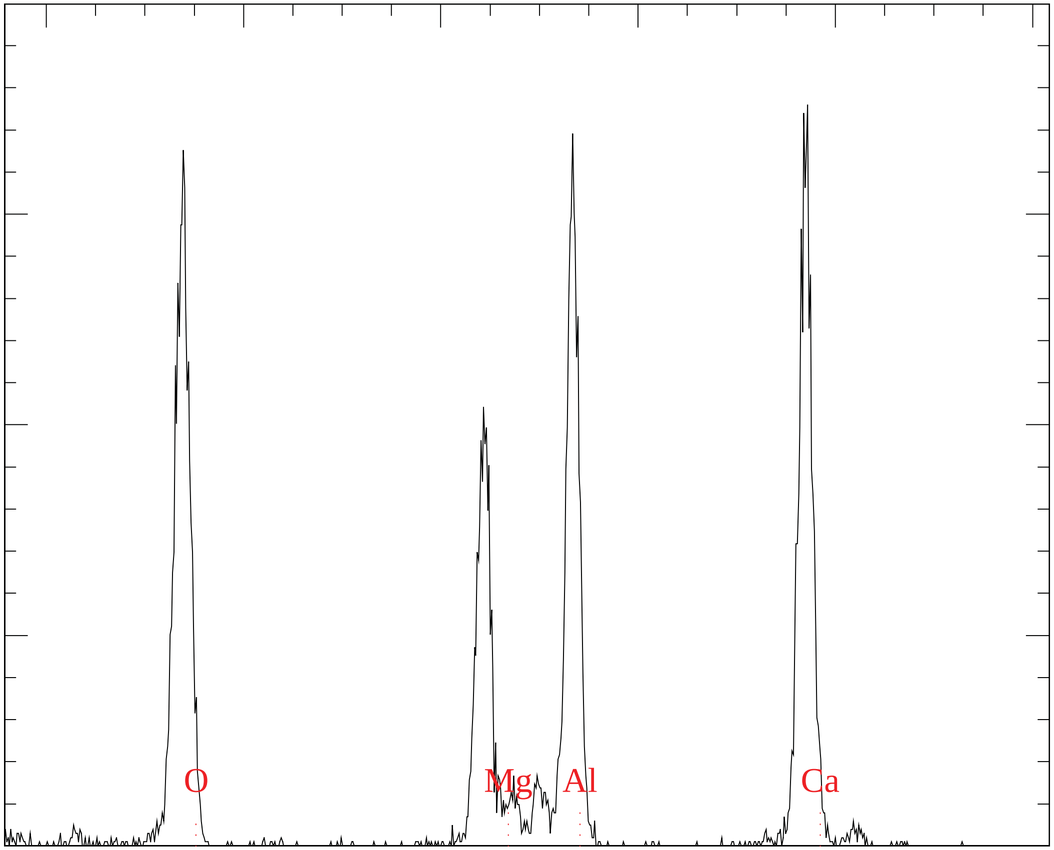


Epitaxial orientation :
(Ca,Mg)O(111) // GaN (0001)



**Beam Direction [11-20]**

# Composition of (Ca,Mg)O by RBS on Carbon Substrates

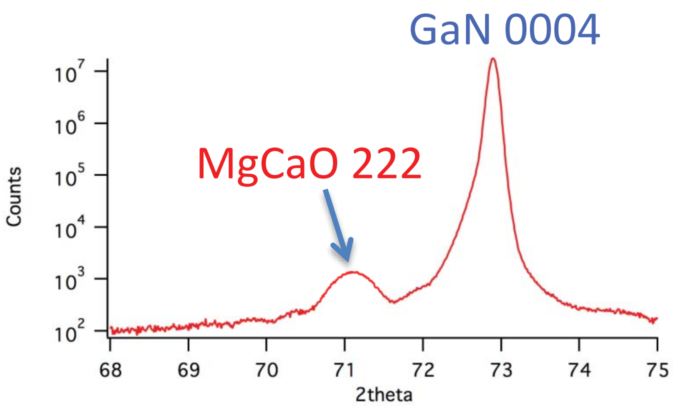


Aluminum in capping layer of ALD $Al_2O_3$

# Lattice Constant Mismatch

Dosing ratio Mg:Ca=1:3;   RBS: Mg:Ca=1:3

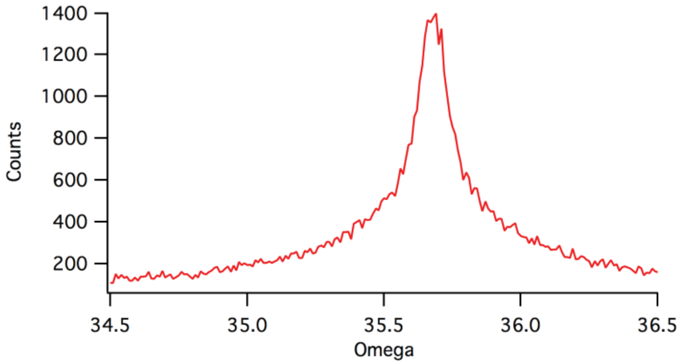
2theta
Omega
scan



too much Ca for
perfect lattice match

2theta=71.09 d=1.325nm  mismatch = 2.2%
(Vegard's law prediction: mismatch = 3.7%)

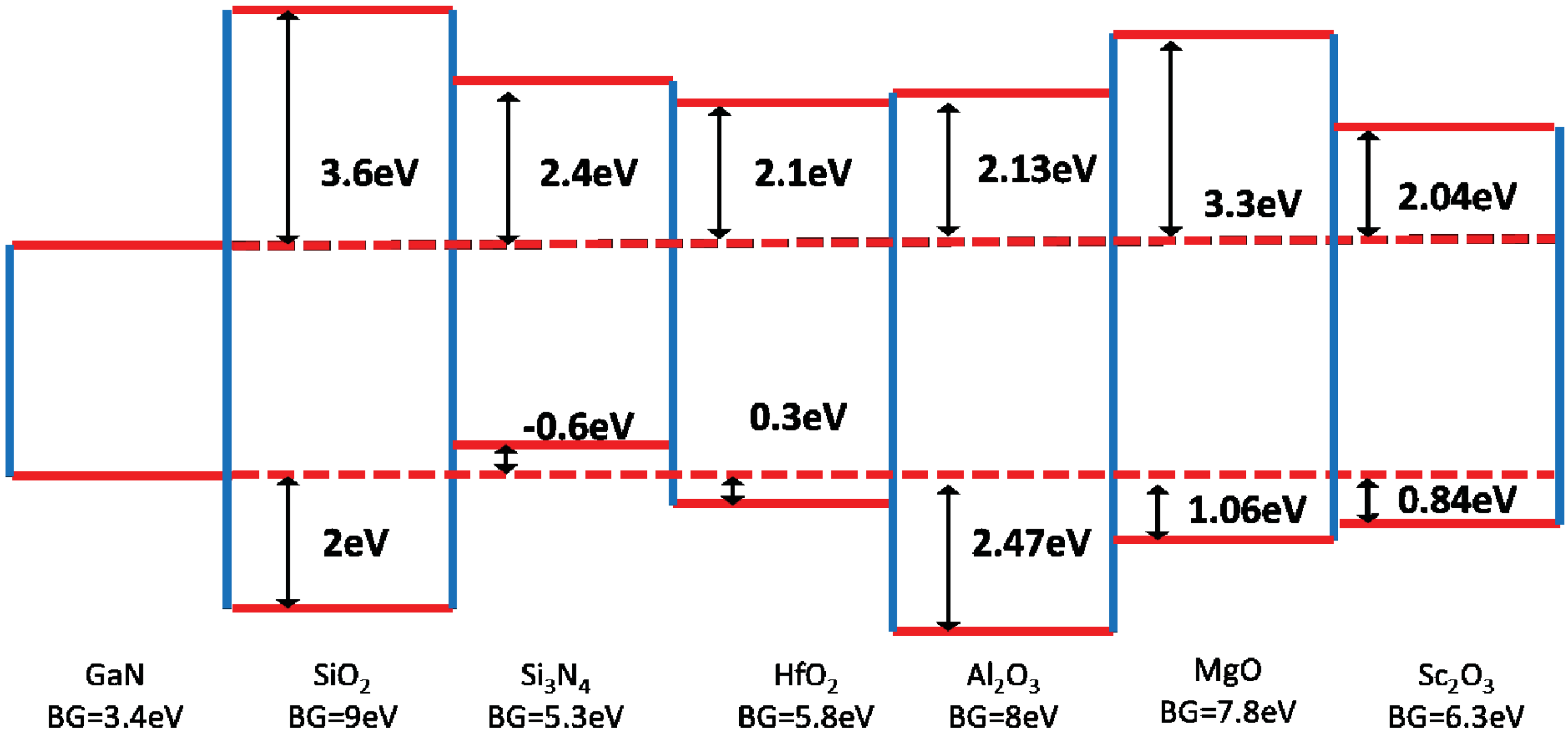
Rocking
scan



FWHM=0.23deg

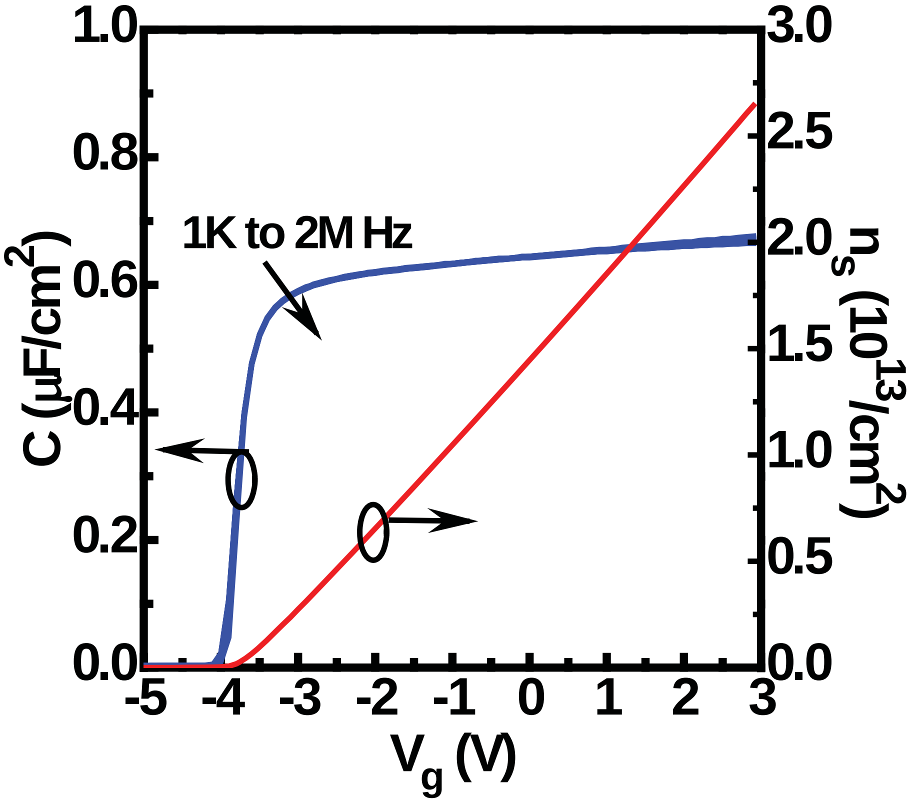
# (Ca,Mg)O is a good insulator on GaN or InAlN

Large band offsets for both conduction and valence bands of MgO

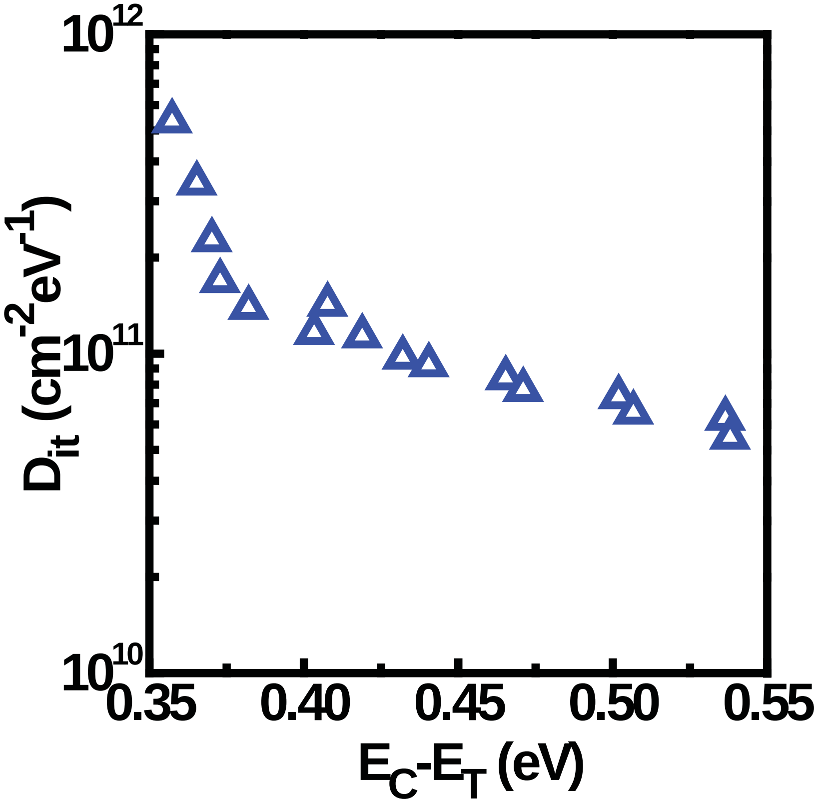


*Materials* **2012**, *5*, 1297-1335

# Capacitor with (Mg,Ca)O on InAlN => Very Few Traps



Almost no frequency dispersion
=> few states at the interface.

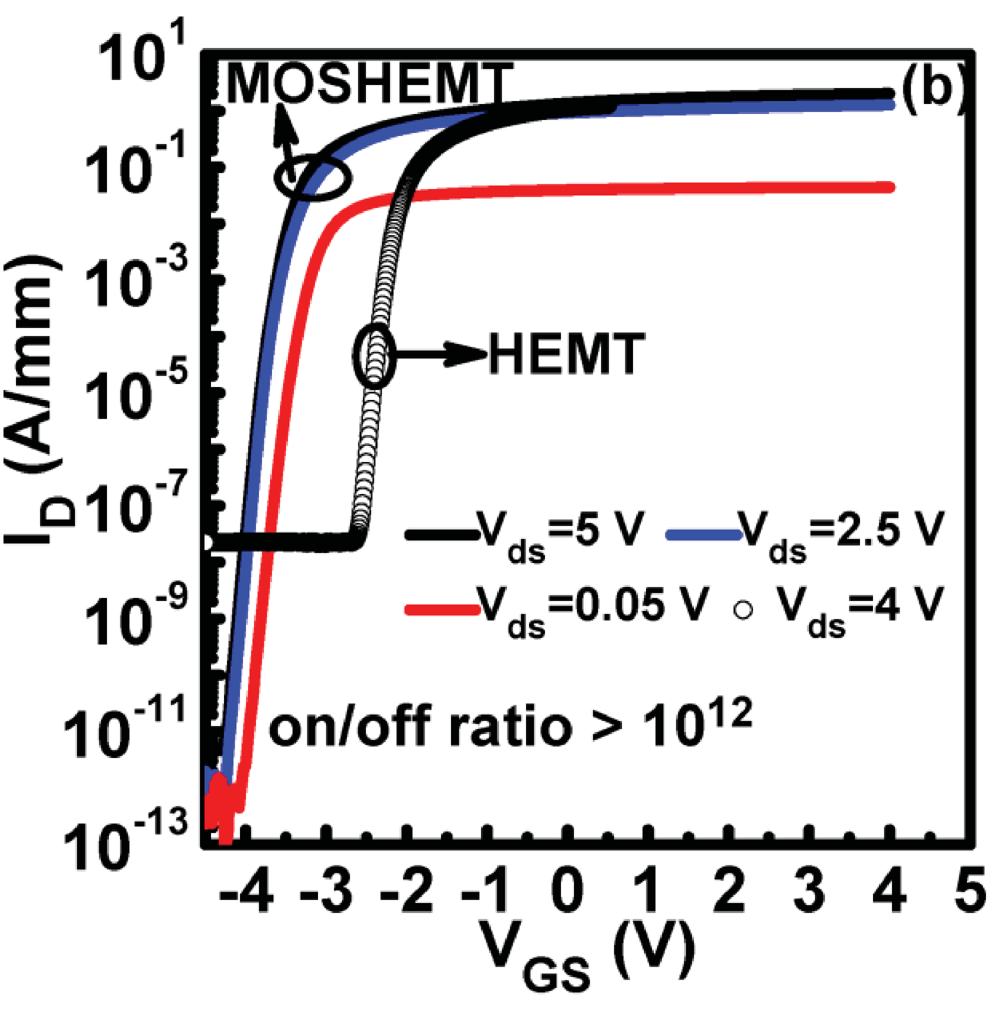


AC conductance extracts very low $D_{it}$
in the bandgap, around $10^{11}$ cm$^{-2}$

# Drain Current vs. Gate Voltage for InAlN Transistors

The (Mg,Ca)O gate insulator reduced the gate leakage by four orders of magnitude, from $10^{-8}$ to $10^{-12}$ A/mm.

The subthreshold slope is nearly ideal at 64 mV/dec.



# Summary

Atomic Layer Epitaxy (ALE) forms high-quality epitaxial interfaces

ALE $La_2O_3$/GaAs(111) => both p- and n- type capacitors with low dispersion

=> the first CMOS circuits with both channels in GaAs

ALE $La_2O_3$/Ge(111) => epitaxial structures

ALE (Mg,Ca)O/GaN or InAlN => capacitors with low dispersion

ALE (Mg,Ca)O/InAlN => transistors with low gate leakage

ALE is a scalable process for making high-performance devices

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DOW

APPLIED MATERIALS

imec

IBM

Harvard University Center for Nanoscale Systems

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