High-Performance InAlN/GaN MOSHEMTs Enabled by Atomic Layer Epitaxy MgCaO as Gate Dielectric

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***Abstract*— We have demonstrated high-performance InAlN/GaN MOS high-electron-mobility-transistors (MOSHEMTs) with various channel lengths (L_{ch}) of 85–250 nm using atomic-layer-epitaxy (ALE) crystalline $Mg_{0.25}Ca_{0.75}O$ as gate dielectric. With a nearly lattice matched epitaxial oxide, the interface between oxide and barrier is improved. The gate leakage current of MOSHEMT is reduced by six orders of magnitude compared with HEMT. An OFF-state leakage current of 3×10^{-13} A/mm, ON/OFF ratio of 4×10^{12}, almost ideal subthreshold swing of 62 mV/decade, low drain current noise with Hooge parameter of 10^{-4}, and negligible current collapse and hysteresis are realized. The 85-nm L_{ch} MOSHEMT also exhibits good ON-state performance with $I_{dmax} = 2.25$ A/mm, $R_{ON} = 1.3\ \Omega \cdot$ mm, and $g_{max} = 475$ mS/mm, showing that ALE MgCaO is a promising gate dielectric for GaN device applications.**

***Index Terms*— InAlN/GaN, MOSHEMT, ALE, epitaxial oxide.**

I. Introduction

RECENTLY, GaN-based high-electron-mobility-transistors (HEMTs) have attracted enormous attention in the areas of high frequency [1]–[3], high power [4], high voltage switching [5] and low noise [6] applications. The lattice-matched InAlN/GaN HEMT structure provides a higher two-dimensional electron gas (2DEG) density than AlGaN/GaN structures due to a larger spontaneous polarization difference between the barrier and channel, and minimized short-channel-effects due to a thinner barrier. However, due to its limited Schottky barrier height and thinner barrier, devices suffer from high gate leakage (I_g), resulting in low forward gate bias swing and poor off-state performance. In this case, metal-oxide-semiconductor HEMTs (MOSHEMTs) are proposed with a thin epitaxial oxide layer in between gate and barrier to solve the aforementioned two problems [7]. The MOSHEMT turns out to be an effective way to suppress gate leakage and passivate the surface in the gate-source and gate-drain regions at the same time.

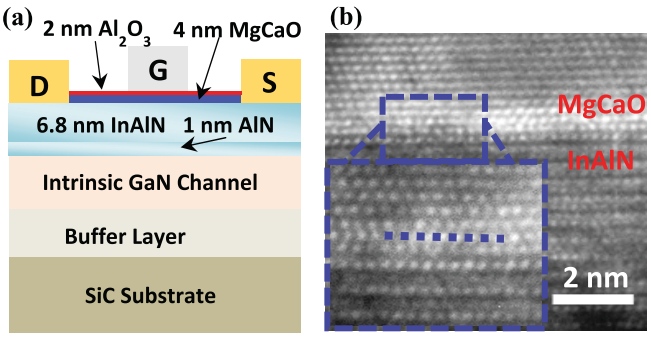

Fig. 1. (a) Schematic of a GaN MOSHEMT and (b) TEM view of the epitaxial MgCaO on InAlN barrier.

Some progresses have been made on GaN MOSHEMTs, and many gate oxides/dielectrics have been investigated, such as SiO_2 [8], SiN [9], [10], Al_2O_3 [11]–[14], HfO_2 [15], La_2O_3 [16], $LaLuO_3$ [17] and AlN [18]. Although the gate leakage is improved, most of them only yield drain current on/off ratios of 10^7-10^{10}, much lower than expected when considering the wide bandgap nature of GaN (3.4 eV). One reason is relatively poor interface between oxide and barrier. In addition, those interface defects also degrade the device low frequency noise performances, with Hooge parameters usually within the range of 10^{-2}-10^{-3} [19], [20]. In this letter, we have demonstrated a latticed-matched epitaxial MgCaO on the InAlN/GaN MOSHEMT with improved on/off ratio exceeding 10^{12} and reduced Hooge parameter of 10^{-4}.

II. Device Fabrication and Measurement

Fig. 1 shows a schematic view of an InAlN/GaN MOSHEMT on a SiC substrate. The barrier is undoped InAlN and the buffer is undoped GaN without back barrier. It has a sheet resistance (R_{sh}) of 260 Ω/□, a 2-dimensional electron gas density of 2×10^{13} cm^{-2} and mobility of 1200 cm^2/V · s, determined by Hall measurement with ALE passivation. Device fabrication started with mesa isolation by Cl_2/BCl_3 etching to a depth of 150 nm. Then, Ohmic contacts were formed by depositing Ti/Al/Au (15/60/50 nm) followed by

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775 °C rapid thermal anneal in N_2 atmosphere, yielding a contact resistance (R_c) of 0.3 $\Omega \cdot$ mm. After that, the wafer was pretreated by diluted BOE (BOE:H_2O=1:5) for 30 s to remove native oxides followed by soaking sample in the NH_4OH solution for 10 min for surface passivation. 4 nm of epitaxial $Mg_{0.25}Ca_{0.75}O$ capped with 2 nm of amorphous Al_2O_3 were then deposited by ALE. The Al_2O_3 is used as capping layer to avoid MgCaO absorbing water in the following processes. The growth temperature of MgCaO was 310 °C, using bis (*N,N'*-di-*tert*-butylacetamidinato) calcium, bis(*N,N'*-di-*sec*-buty lacetamidinato)magnesium, and water vapor as precursors [21]. The ratio of Mg and Ca is controlled by alternating between 1 cycle of MgO and 3 cycles of CaO. A high-resolution TEM image of ALE MgCaO on the InAlN barrier confirms the epitaxial structure of MgCaO as shown in Fig. 1(b). The success of epitaxial growth is based on the similar hexagonal lattice of MgCaO (111) crystal orientation and InAlN (0001) surface of wurtzite structure. There is only 1.5% lattice mismatch between the MgCaO and the InAlN barrier, determined by X-ray diffraction (XRD) experiment, which provides a high-quality oxide/InAlN interface. Finally, 30 nm of Ni were deposited as the gate metal followed by lift-off process. All the lithography processes were carried out using a Vistec VB6 e-beam lithography system.

All the devices have a gate width of 20 μm, scaled channel lengths (L_{ch}) of 85-250 nm and a source to drain spacing (L_{sd}) of 1 μm. The gate is centered between the source and drain. The DC measurements were carried out with Keithley 4200 Semiconductor Characterization System at room temperature. The noise measurements were performed by using current amplifier and digital signal analyzer [22].

III. Results and Discussion

Fig. 2(a) shows the well-behaved output characteristics (I_d-V_{ds}) of a GaN MOSHEMT with L_{ch} = 85 nm and L_{sd} = 1 μm. Due to a 6 nm thick gate oxide, a high forward gate bias (V_{gs}) of 4 V is applied and thereby a maximum drain current (I_{dmax}) of 2.25 A/mm is realized at V_{ds} = 9 V. The on-resistance (R_{on}) of 1.3 $\Omega \cdot$ mm is extracted from linear region of I_d-V_{ds}. Fig. 2 (b) depicts the transconductance (g_m) and I_d transfer plot in the linear region with V_{gs} biased from -5 V to 4 V. Despite a wide gate to channel spacing, the GaN MOSHEMT still exhibits a peak extrinsic g_m (g_{max}) of 475 mS/mm at I_d = 350 mA/mm and V_{ds} = 5 V. The threshold voltage (V_T) is obtained from linear extrapolation of the drain current from the point of peak transconductance, yielding $V_T = -3.65$ V at V_{ds} = 5 V.

Fig. 2(c) is the transfer characteristic at the log-scale plot at V_{ds} = 2.5 V and 5 V. Even with a 85 nm L_{ch}, this device still has a ultra-high on/off ratio of 4×10^{12} and 4×10^{11} for V_{ds} = 2.5 V and 5 V, respectively. Traditional HEMT devices are not able to have such a high on/off ratio because of their large gate leakage currents (I_g) in the off-state. The I_g of the MOSHEMT at off-state is 10^{-12} to 10^{-13} A/mm, which is reduced by 6 orders compared with the I_g of a HEMT with the same structure. The MgCaO has conduction band offset of greater than 2 eV with respect to the InAlN barrier [23], allowing 4 nm of MgCaO and 2 nm of Al_2O_3 to provide enough barrier height to minimize the tunneling current from the gate electrode to the 2DEG channel. The high on/off ratio also indicates a high quality oxide/barrier interface, otherwise the channel would not be depleted completely at the off-state.

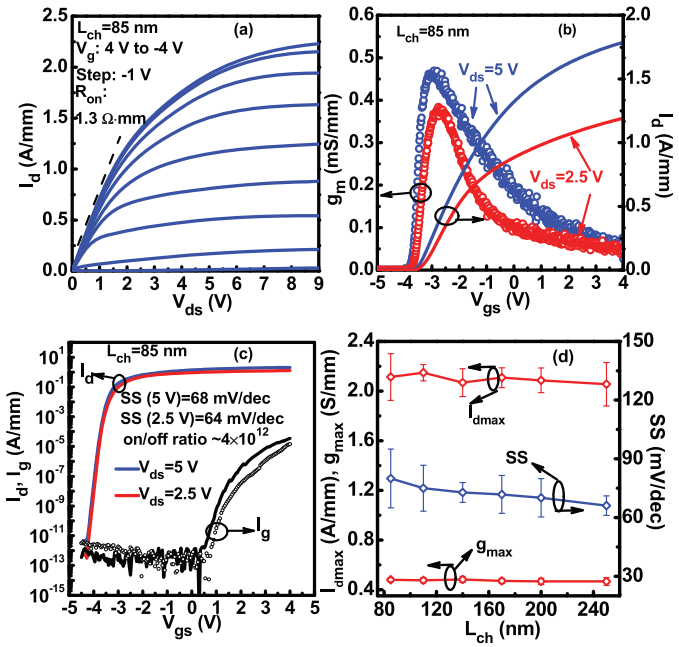

Fig. 2. (a) Output characteristics (L_{ch} = 85 nm) when V_g varies from 4 V to −5 V with −1 V as step. (b) g_m-V_{gs} and I_d-V_{gs} transfer characteristics of the same device at linear region plot. (c) I_d-V_{gs} transfer characteristics at the log-scale plot with high on/off ratio of 4×10^{12} and low SS of 64 mV/dec. The solid I_g-V_{gs} curve is measured at V_{ds} = 2.5V, while dotted curve is measured at V_{ds} = 5V. (d) I_{dmax}, g_{mmax} and SS (V_{ds} = 5 V) scaling metrics when L_{ch} is from 85 nm to 250 nm.

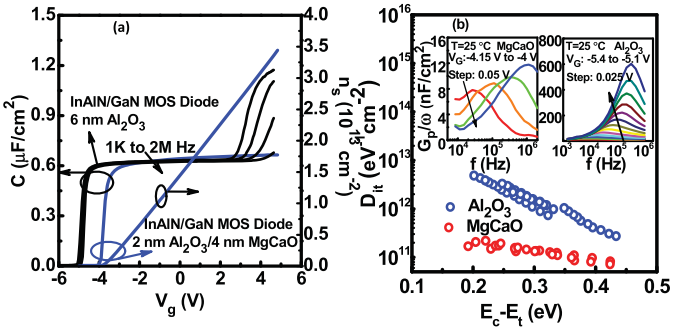

Fig. 3. (a) C-V comparison between Al_2O_3/InAlN/GaN and MgCaO/InAlN/GaN MOS diode and 2DEG density ~V_g at room T and (b) D_{it} distributions in the bandgap for both MgCaO and Al_2O_3 samples. Insets are the typical Gp/ω peaks for MgCaO and Al_2O_3 samples at T = 25°C.

In addition to the ultra-high on/off ratio, the MOSHEMT also has a low substhreshold swing (SS) of 64 and 68 mV/dec for V_{ds} = 2.5 V and 5 V, respectively. The low SS is mostly from the high quality interface, low equivalent oxide thickness, and ultra-thin thickness of the 2DEG.

Fig.2 (d) describes the I_{dmax}, g_{max} and SS scaling behavior of GaN MOSHEMTs with L_{ch} of 85-250 nm. Each error bar is the standard deviation of 6 devices on the same chip. On-state performance weakly improves with L_{ch} scales from 250 nm down to 85 nm, since L_{sd} is much larger than L_{ch}. SS is increased when L_{ch} is scaled, which shows the typical short channel effect. The minimum SS achieved is 62 mV/dec for both forward and reverse sweep. The short channel effects can be further reduced by improving the confinement of the 2DEG in the channel by adding back barriers [24].

Fig. 3(a) shows measured room temperature capacitance-voltage (C-V) at the frequency (f) of 1 K to 2 MHz. The Al_2O_3/MgCaO/InAlN MOS capacitor has a diameter of 75μm.

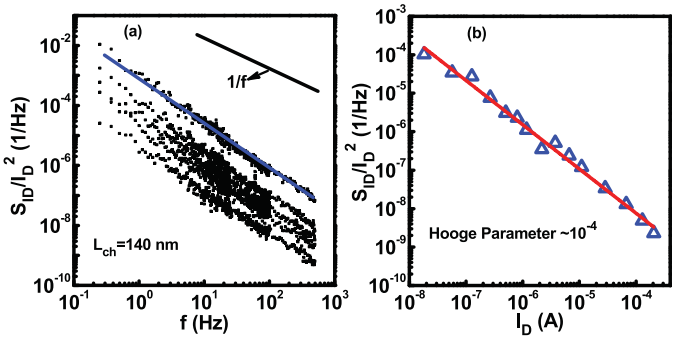

Fig. 4. Normalized power spectral density with (a) various V_g and (b) drain current at f = 10 Hz.

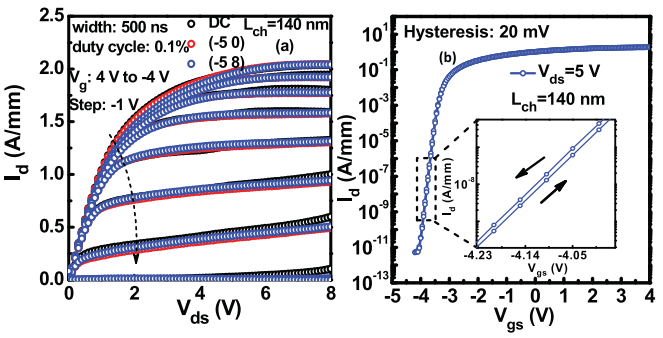

Fig. 5. (a) Pulsed I-V measurements with 500 ns pulse width and 0.1% duty cycle and (b) I_d-V_{gs} hysteresis of a MOSHEMT with L_{ch} = 140 nm.

As shown in the Fig. 3(a), there is almost zero frequency dispersion in the typical frequency ranges. The dielectric constant of MgCaO is calculated to be ∼10 by subtracting the capacitance of the InAlN barrier. By integration of the C-V curve from depletion to accumulation, we can get an ultra-high electron density of 3.5×10^{13} cm^{-2} at $V_g = 5$ V. Note that we don't observe a second sharp increase of the capacitance until we increase V_g to 5 V, shortly before the oxide failed at $V_g = 5.5$ V. The second sharp increase is observed in the oxide (or insulator)/AlGaN systems [13], [16], [25], caused by electrons in the 2DEG channel spilling into barrier. The second capacitance increase is also observed in InAlN MOSHEMT when 2DEG density is up to 1.4×10^{13} cm^{-2} [26]. In our devices, we suggest that the negligible introduction of the extra positive charge at the oxide/barrier interface is attributed to the suppression of the 2nd capacitance increase before $V_g = 5$ V. The oxide/barrier positive charge will help to pull down the conduction band of the barrier so that electrons will be easier to spill over the barrier to the oxide/barrier interface to induce the 2nd C-V step. This positive charge is typically observed at the ALD amorphous oxide/barrier interface [11], [27], [28]. To prove this suggestion, we also fabricated ALD amorphous Al_2O_3/InAlN/GaN MOS capacitor with 6 nm of Al_2O_3. Compared with C-V curve of previous MgCaO/InAlN/GaN MOS capacitor, the latter one shows a negatively shifted V_T and a 2nd C-V step. The negatively shifted V_T confirms the existence of the positive charges at Al_2O_3/InAlN interface, which finally induces the 2nd C-V step as aforementioned. In our case, MgCaO can effectively confine electrons in the channel even at a high 2DEG density of 3.5×10^{13} cm^{-2}. This is very favorable to the device operation since electrons will have a much higher mobility in the low bandgap GaN layer compared with a lower mobility in a wider bandgap InAlN layer. Meanwhile, we also carried out AC conductance measurements to extract the *measured overall* interface trap density (D_{it}) from 25 °C to 150 °C for both MgCaO and Al_2O_3 devices as shown in Fig. 3(b). The extracted D_{it} is within the range of 0.5 to 3.4×10^{11} cm^{-2}eV^{-1} for the MgCaO sample and 0.3 to 6.0×10^{12} cm^{-2}eV^{-1} for the Al_2O_3 sample. Note that the *measured overall* D_{it} is neither simply from the dielectric/InAlN interface nor from the InAlN/GaN interface. More experiments and modeling work are needed to distinguish the traps from two different interfaces in the complex GaN MOSHEMT structures.

To analyze the trapping and detrapping phenomena in InAlN/GaN MOSHEMT, 1/f low noise spectra with various drain currents are also measured. Fig. 4 shows the normalized power spectral density with various V_g and drain current at f = 10 Hz, $V_{ds} = 0.05$ V and $L_{ch} = 140$ nm. The Hooge parameter (α_H) is calculated to be $\sim 10^{-4}$ by using following equation [29]:

$$\alpha_H = \frac{S_{IDS} \times f \times L_g^2}{I_{DS} \times q \times \mu \times V_{DS}}$$

where q is the elementary electron charge and μ is the electron mobility of 1200 cm^2/V · s. The α_H of our epitaxial oxide MOSHEMT is comparable to the HEMT ($\sim 10^{-4}$) [30], [31]. On the other hand, MOSHEMTs with amorphous gate dielectric usually suffer from relatively high oxide/barrier interface state densities. The carrier trapping between the oxide and barrier resulted in the increase of α_H, with general α_H value of $10^{-3} \sim 10^{-2}$. The one or two order of magnitudes lower α_H of epitaxial oxide MOSHEMT is consistent with near zero frequency dispersion C-V data and also further confirms that our lattice-matched epitaxial oxide has an unprecedented high quality interface with the InAlN barrier.

Fig. 5(a) is the pulsed I-V measurement of the device with $L_{ch} = 140$ nm. The pulse width and pulse period are 500 ns and 500 μs, respectively. The quiescent bias points are set at $(V_{GSQ}, V_{DSQ}) = (-5, 0)$ and $(-5, 8)$ for gate and drain pulse, respectively. Effective suppression of the current collapse by MgCaO is demonstrated with little difference between the DC and gate and drain pulsed drain currents. Fig. 5(b) is the I_d-V_{gs} hysteresis measurement of the same device. A negligible hysteresis of 20 mV is observed when V_g is sweeping from $V_g = -4.5$ to 4 V and then sweeping back, which further confirms an ultra-high quality interface between MgCaO and InAlN barrier.

IV. Conclusion

We have experimentally demonstrated an epitaxial oxide InAlN/GaN MOSHEMT by using ALE technique. Benefiting from a lattice-matched interface, the off-state drain leakage current is reduced to 3×10^{-13} A/mm, yielding a high drain current on/off ratio of 4×10^{12}. A low Hooge parameter of 10^{-4} is obtained, showing the high quality interface between epitaxial oxide MgCaO and InAlN barrier. In addition, pulse and hysteresis measurements reveal that the current collapse and hysteresis are suppressed. Combined with the high device performance of $I_{dmax} = 2.25$ A/mm, $R_{on} = 1.3\ \Omega \cdot$ mm, and $g_{max} = 475$ mS/mm, the MgCaO MOSHEMT turns out to be a good candidate for GaN device applications.

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REFERENCES

[1] K. Shinohara, D. Regan, A. Corrion, D. Brown, S. Burnham, P. J. Willadsen, I. Alvarado-Rodriguez, M. Cunningham, C. Butler, A. Schmitz, S. Kim, B. Holden, D. Chang, V. Lee, A. Ohoka, P. M. Asbeck, and M. Micovic, "Deeply-scaled self-aligned-gate GaN DH-HEMTs with ultrahigh cutoff frequency," in *IEDM Tech. Dig.*, 2011, pp. 19.1.1–19.1.4, doi: 10.1109/IEDM.2011.6131582.

[2] Y. Yue, Z. Hu, J. Guo, B. Sensale-Rodriguez, G. Li, R. Wang, F. Faria, T. Fang, B. Song, X. Gao, S. Guo, T. Kosel, G. Snider, P. Fay, D. Jena, and H. Xing, "InAlN/AlN/GaN HEMTs with regrown ohmic contacts and f_T of 370 GHz," *IEEE Electron Device Lett.*, vol. 33, no. 7, pp. 988–990, Jul. 2012, doi: 10.1109/LED.2012.2196751.

[3] D. S. Lee, X. Gao, S. Guo, D. Kopp, P. Fay, and T. Palacios, "300-GHz InAlN/GaN HEMTs with InGaN back barrier," *IEEE Electron Device Lett.*, vol. 32, no. 11, pp. 1525–1527, Nov. 2011, doi: 10.1109/LED.2011.2164613.

[4] Y.-F. Wu, A. Saxler, M. Moore, R. P. Smith, S. Sheppard, P. M. Chavarkar, T. Wisleder, U. K. Mishra, and P. Parikh, "30-W/mm GaN HEMTs by field plate optimization," *IEEE Electron. Device Lett.*, vol. 25, no. 3, pp. 117–119, Mar. 2004, doi: 10.1109/LED.2003.822667.

[5] J. Derluyn, M. Van Hove, D. Visalli, A. Lorenz, D. Marcon, P. Srivastava, K. Geens, B. Sijmus, J. Viaene, X. Kang, J. Das, F. Medjdoub, K. Cheng, S. Degroote, M. Leys, G. Borghs, and M. Germain, "Low leakage high breakdown E-mode GaN DHFET on Si by selective removal of *in-situ* grown Si_3N_4," in *IEDM Tech. Dig.*, Dec. 2009, pp. 1–4, doi: 10.1109/IEDM.2009.5424399.

[6] Z. H. Liu, S. Arulkumaran, and G. I. Ng, "Improved microwave noise performance by SiN passivation in AlGaN/GaN HEMTs on Si," *IEEE Microw. Wireless Compon. Lett.*, vol. 19, no. 6, pp. 383–385, Jun. 2009, doi: 10.1109/LMWC.2009.2020027.

[7] P. D. Ye, B. Yang, K. K. Ng, J. Bude, G. D. Wilk, S. Halder, and J. C. M. Huang, "GaN metal-oxide-semiconductor high-electron-mobility-transistor with atomic layer deposited Al_2O_3 as gate dielectric," *Appl. Phys. Lett.*, vol. 86, no. 6, pp. 063501-1–063501-3, Feb. 2005, doi: 10.1063/1.1861122.

[8] F. Husna, M. Lachab, M. Sultana, V. Adivarahan, Q. Fareed, and A. Khan, "High-temperature performance of AlGaN/GaN MOSHEMT with SiO_2 gate insulator fabricated on Si (111) substrate," *IEEE Trans. Electron Device*, vol. 59, no. 9, pp. 2424–2429, Sep. 2012. doi: 10.1109/TED.2012.2204888.

[9] V. Adivarahan, M. Gaevski, W. H. Sun, H. Fatima, A. Koudymov, S. Saygi, G. Simin, J. Yang, M. A. Khan, A. Tarakji, M. S. Shur, and R. Gaska, "Submicron gate Si_3N_4/AlGaN/GaN-metal-insulator-semiconductor heterostructure field-effect transistors," *IEEE Electron Device Lett.*, vol. 24, no. 9, pp. 541–543, Sep. 2003, doi: 10.1109/LED.2003.816574.

[10] D. Denninghoff, J. Lu, M. Laurent, E. Ahmadi, S. Keller, and U. Mishra, "N-polar GaN/InAlN MIS-HEMT with 400-GHz f_{max}," in *Proc. 70th Annu. Device Res. Conf.*, Jun. 2012, pp. 151–152, doi: 10.1109/DRC.2012.6256939.

[11] Z. Hu, Y. Yue, M. Zhu, B. Song, S. Ganguly, J. Bergman, D. Jena, and H. G. Xing, "Impact of CF_4 plasma treatment on threshold voltage and mobility in Al_2O_3/InAlN/GaN MOSHEMTs," *Appl. Phys. Exp.*, vol. 7, pp. 031002-1–031002-4, Feb. 2014, doi: 10.7567/APEX.7.031002.

[12] J. J. Freedsman, T. Kubo, and T. Egawa, "High drain current density E-mode Al_2O_3/AlGaN/GaN MOS-HEMT on Si with enhanced power device figure-of-merit ($4 \times 10^8 V^2 \Omega^{-1} cm^{-2}$)," *IEEE Trans. Electron Devices*, vol. 60, no. 10, pp. 3079–3083, Oct. 2013, doi: 10.1109/TED.2013.2276437.

[13] S. Yang, Z. Tang, K.-Y. Wong, Y.-S. Lin, Y. Lu, S. Huang, and K. J. Chen, "Mapping of interface traps in high-performance Al_2O_3/AlGaN/GaN MIS-heterostructures using frequency- and temperature-dependent C-V techniques," in *IEDM Tech. Dig.*, Dec. 2013, pp. 6.3.1–6.3.4, doi: 10.1109/IEDM.2013.6724573.

[14] D. Xu, K. K. Chu, J. A. Diaz, M. Ashman, J. J. Komiak, L. M. Pleasant, C. Creamer, K. Nichols, K. H. G. Duh, P. M. Smith, P. C. Chao, L. Dong, and P. D. Ye, "0.1-μm atomic layer deposition Al_2O_3 passivated InAlN/GaN high electron-mobility transistors for E-band power amplifiers," *IEEE Electron Device Lett.*, vol. 36, no. 5, pp. 442–444, May 2015, doi: 10.1109/LED.2015.2409264.

[15] X. Sun, O. I. Saadat, K. S. Chang-Liao, T. Palacios, S. Cui, and T. P. Ma, "Study of gate oxide traps in HfO_2/AlGaN/GaN metal-oxide-semiconductor high-electron-mobility transistors by use of AC transconductance method," *Appl. Phys. Lett.*, vol. 102, pp. 103504-1–103504-4, Mar. 2013, doi: 10.1063/1.4795717.

[16] H.-C. Chiu, C.-W. Lin, C.-H. Chen, C.-W. Yang, C.-K. Lin, J. S. Fu, L.-B. Chang, R.-M. Lin, and K.-P. Hsueh, "Low hysteresis dispersion La_2O_3 AlGaN/GaN MOS-HEMTs," *J. Electrochem. Soc.*, vol. 157, no. 2, pp. H160–H164, 2010, doi: 10.1149/1.3264622.

[17] S. Yang, S. Huang, H. Chen, C. Zhou, Q. Zhou, M. Schnee, Q.-T. Zhao, J. Schubert, and K. J. Chen, "AlGaN/GaN MISHEMTs with high-κ $LaLuO_3$ gate dielectric," *IEEE Electron Device Lett.*, vol. 33, no. 7, pp. 979–981, Jul. 2012, doi: 10.1109/LED.2012.2195291.

[18] S. Liu, S. Yang, Z. Tang, Q. Jiang, C. Liu, M. Wang, and K. J. Chen, "Al_2O_3/AlN/GaN MOS-channel-HEMTs with an AlN interfacial layer," *IEEE Electron Device Lett.*, vol. 35, no. 7, pp. 723–725, Jul. 2014, doi: 10.1109/LED.2014.2322379.

[19] H.-C. Chiu, J.-H. Wu, C.-W. Yang, F.-H. Huang, and H.-L. Kao, "Low-frequency noise in enhancement-mode GaN MOS-HEMTs by using Stacked $Al_2O_3/Ga_2O_3/Gd_2O_3$ gate dielectric," *IEEE Electron Device Lett.*, vol. 33, no. 7, pp. 958–960, Jul. 2012, doi: 10.1109/LED.2012.2194980.

[20] J.-H. Bae, I. Hwang, J.-M. Shin, H.-I. Kwon, C. H. Park, J. Ha, J. Lee, H. Choi, J. Kim, J.-B. Park, J. Oh, J. Shin, U.-I. Chung, and J.-H. Lee, "Characterization of traps and trap-related effects in recessed-gate normally-off AlGaN/GaN-based MOSHEMT," in *IEDM Tech. Dig.*, Dec. 2012, pp. 303–306, doi: 10.1109/IEDM.2012.6479034.

[21] X. Lou, J. Zhang, S. B. Kim, S. Al-Ghamdi, P. D. Ye, and R. G. Gordon, "Epitaxial growth of MgCaO on GaN by atomic layer deposition," to be published.

[22] N. Conrad, M. Si, S. H. Shin, J. J. Gu, J. Zhang, M. A. Alam, and P. D. Ye, "Low-frequency noise and RTN on near-ballistic III–V GAA nanowire MOSFETs," in *IEDM Tech. Dig.*, Dec. 2014, pp. 20.1.1–20.1.4, doi: 10.1109/IEDM.2014.7047086.

[23] J.-J. Chen, M. Hlad, A. P. Gerger, B. P. Gila, F. Ren, C. R. Abernathy, and S. J. Pearton, "Band offsets in the $Mg_{0.5}Ca_{0.5}O$/GaN heterostructure system," *J. Electron. Mater.*, vol. 36, pp. 368–372, Dec. 2006. 10.1007/s11664-006-0037-9.

[24] T. Palacios, A. Chakraborty, S. Heikman, S. Keller, S. P. DenBaars, and U. K. Mishra, "AlGaN/GaN high electron mobility transistors with InGaN back-barriers," *IEEE Electron Device Lett.*, vol. 27, no. 1, pp. 13–15, Jan. 2006, doi: 10.1109/LED.2005.860882.

[25] Y. Hori, Z. Yatabe, and T. Hashizume, "Characterization of interface states in Al_2O_3/AlGaN/GaN structures for improved performance of high-electron-mobility transistors," *J. Appl. Phys.*, vol. 114, no. 24, pp. 244503-1–244503-8, Dec. 2013, doi: 10.1063/1.4859576.

[26] F. Qian, L. Qian, X. Tao, W. Qiang, Z. Jin-Cheng, and H. Yue, "Performance of La_2O_3/InAlN/GaN metal–oxide–semiconductor high electron mobility transistors," *Chin. Phys. B*, vol. 21, no. 6, pp. 067305-1–067305-6, Sep. 2003, doi: 10.1088/1674-1056/21/6/067305.

[27] S. Ganguly, J. Verma, G. Li, T. Zimmermann, H. Xing, and D. Jena, "Presence and origin of interface charges at atomic-layer deposited Al_2O_3/III-nitride heterojunctions," *Appl. Phys. Lett.*, vol. 99, no. 19, p. 193504-1–193504-3, Nov. 2011, doi: 10.1063/1.3658450.

[28] H. Zhou, G. I. Ng, Z. H. Liu, and S. Arulkumaran, "Improved device performance by post-oxide annealing in atomic-layer-deposited Al_2O_3/AlGaN/GaN metal–insulator–semiconductor high electron mobility transistor on Si," *Appl. Phys. Exp.*, vol. 4, no. 10, pp. 104102-1–104102-3, Oct. 2011, doi: 10.1143/APEX.4.104102.

[29] J.-M. Peransin, P. Vignaud, D. Rigaud, and L. K. J. Vandamme, "1/f noise in MODFETs at low drain bias," *IEEE Trans. Electron. Devices*, vol. 37, no. 10, pp. 2250–2253, Oct. 1990. doi: 10.1109/16.59916.

[30] A. V. Vertiatchikh and L. F. Eastman, "Effect of the surface and barrier defects on the AlGaN/GaN HEMT low-frequency noise performance," *IEEE Electron Device Lett.*, vol. 24, no. 9, pp. 535–537, Sep. 2003, doi: 10.1109/LED.2003.816588.

[31] A. Balandin, K. L. Wang, S. Cai, R. Li, C. R. Viswanathan, E. N. Wang, and M. Wojtowicz, "Investigation of flicker noise and deep-levels in GaN/AlGaN transistors," *J. Electron. Mater.*, vol. 29, no. 3, pp. 297–301, 2000, doi: 10.1007/s11664-000-0066-8.