Enhancement-Mode AlGaN/GaN Fin-MOSHEMTs on Si Substrate With Atomic Layer Epitaxy MgCaO

Hong Zhou, Xiabing Lou, Sang Bok Kim, Kelson D. Chabak, Roy G. Gordon, and Peide D. Ye, *Fellow, IEEE*

***Abstract*— We have demonstrated high-performance enhancement-mode or normally-off AlGaN/GaN fin-MOSHEMTs on a Si substrate with various fin width of 100–210 nm using atomic layer epitaxy (ALE) MgCaO as the gate dielectric. Through the fixed negative charges in MgCaO depleting the channel at the fin sidewalls, in contrast to the usual positive charges in atomic layer deposited amorphous Al_2O_3, the threshold voltage (V_T) is positively shifted and normally-off device is realized. A high maximum drain current (I_{DMAX}) of 670 mA/mm, high on/off ratio of $10^{10} \sim 10^{12}$, and V_T of 1 V have been achieved on the device. Combining with negligible I_D–V_{GS} hysteresis of 30 mV and current collapse, the ALE MgCaO fin-MOSHEMT turns out to be a promising candidate for the future GaN power device applications.**

***Index Terms*— GaN, MOSHEMT, epitaxial oxide, E-mode.**

I. Introduction

RECENTLY, GaN HEMTs or MOSHEMTs on Si substrates have attracted enormous attentions in the area of power electronics [1]–[6]. As a promising power switch, it is desired for GaN devices to operate in enhancement (E)-mode condition to satisfy the failure-safe requirement. Nowadays, there are several widely applied approaches to realize E-mode, such as F^- ion implantation, gate recess and utilization of p-type GaN capping layer [7]–[11]. Although some progress has been achieved, there are still some inherent limitations. For instance, the gate recess technique causes V_T non-uniformity across the whole wafer due to the lack of etch-stop layers on GaN and it also degrades the electron mobility (μ) because of etch damage to the barrier. Some other methods utilize the work function difference between the metal gate and GaN channel, so that a fin-HEMT and fin-MOSHEMT with narrow fin width can also achieve the E-mode operation [12]–[15]. However, their maximum drain current (I_{DMAX}) is usually limited, mostly likely due to the transport quality of 2-dimensional-electron-gas (2DEG) is degraded since it is too close to the fin sidewalls with increased surface roughness from the sidewall etching.

In our previous works, we have noticed that there are significant negative charges built in at the MgCaO/GaN interface, compared to Al_2O_3 with positive charges at the interface [16]. By combining the negative charges and fin structures, the 2DEG channel can be further depleted, thereby shifting V_T from negative in the planar devices to positive in the fin-MOSHEMTs. Since MgCaO contains built in negative charges, the V_T non-uniformity can be resolved by accurately controlling the MgCaO thickness from ALD cycles. The fin width can be much wider than aforementioned cases due to the existence of negative charges in ALE MgCaO [12]–[15]. The electron μ degradation can also be mitigated by the wider fin structures. The 2DEG mobility of a wider fin can be much higher than that of a narrower fin structure, since most of the 2DEG channel is far from the side walls and thus μ sustains.

In this work, high I_{DMAX}, high on/off ratio, negligible hysteresis, and negligible current collapse show the great promise to apply high-performance ALE MgCaO normally-off fin-MOSHEMTs in future power electronics applications.

II. Device Fabrication and Measurement

The AlGaN/GaN epitaxy substrate was grown on a Si substrate, consisting of, a 17-nm $Al_{0.26}Ga_{0.74}N$ barrier, a 1-nm AlN spacer, a GaN channel, and a 600-nm GaN buffer. Fig. 1(a) shows schematic top and cross-sectional view of AlGaN/GaN fin-MOSHEMT on Si substrate. Device fabrication started with mesa isolation by Cl_2/BCl_3 etching to a depth of 80 nm. Then, Ohmic contacts were formed by depositing Ti/Al/Ni/Au (20/100/40/50 nm) followed by 775 °C rapid thermal anneal in N_2 atmosphere. Sheet resistance (R_{SH}) and contact resistance (R_C) were determined to be 450 Ω/□ and 0.3 Ω·mm through transfer length method (TLM). Various fin widths from 100 nm to 210 nm were then patterned followed by Cl_2/BCl_3 dry etching. 3 minutes of O_2 plasma was used to smooth the sidewall surface and remove etching damage. Prior to the oxide deposition, native oxide was etched by diluted BOE (BOE:H_2O = 1:5) for 30 s followed by soaking sample in NH_4OH solution for 10 min for surface cleaning. 7 nm of epitaxial $Mg_{0.25}Ca_{0.75}O$ followed with 33 nm of amorphous

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H. Zhou and P. D. Ye are with the School of Electrical and Computer Engineering and Birck Nanotechnology Center, Purdue University, West Lafayette, IN 47907 USA (e-mail: yep@purdue.edu).

X. Lou, S. B. Kim, and R. G. Gordon are with the Department of Chemistry and Chemical Biology, Harvard University, Cambridge, MA 02138 USA.

K. D. Chabak is with the Air Force Research Laboratory, Sensors Directorate, Wright-Patterson Air Force Base, Dayton, OH 45433 USA.

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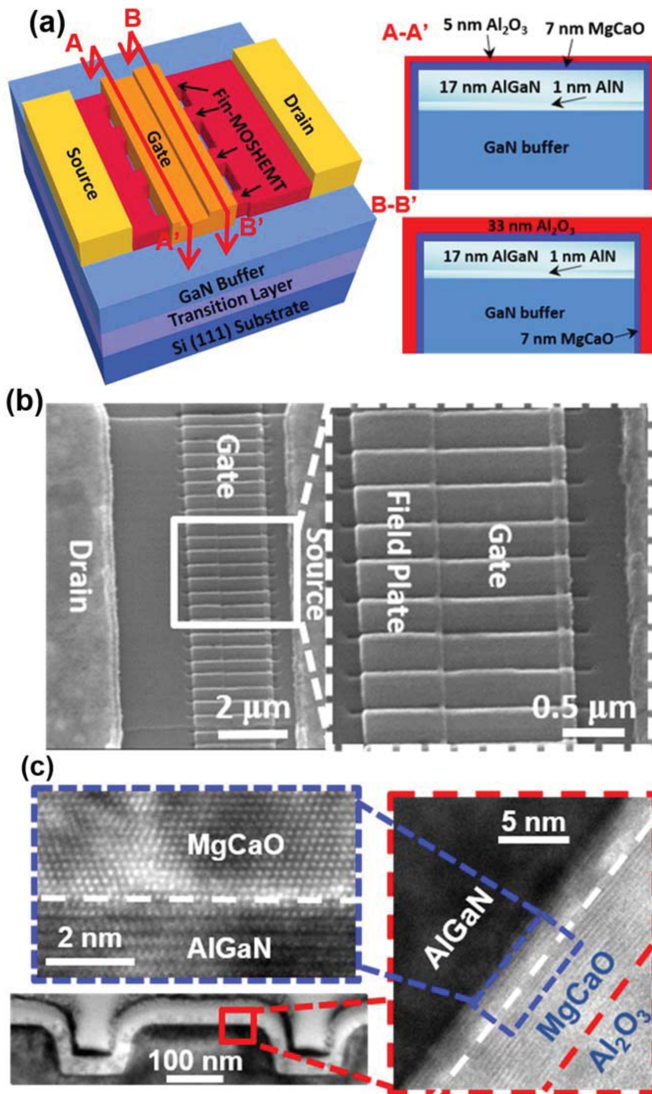

Fig. 1. (a) Schematic of a GaN fin-MOSHEMT, (b) SEM image of a fabricated GaN fin-MOSHEMT with W_{fin} = 210 nm and (c) High resolution TEM image of epitaxy MgCaO on AlGaN.

Al_2O_3 were deposited in one ALD chamber. The Al_2O_3 is used as a capping layer to avoid MgCaO absorbing water in the following process. A bilayer of 7 nm MgCaO and 5 nm Al_2O_3 is used as the gate oxide and a bilayer of 7 nm MgCaO and 33 nm Al_2O_3 is used as the fin extension field plate oxide. 5 nm of Al_2O_3 is achieved through the recess of 33 nm Al_2O_3 by dry etching using a combination of BCl_3 and Ar gases.

Then post deposition annealing at 500 °C for 1 min under O_2 atmosphere was used to further improve the oxide and interface quality. Finally, gate electrode was deposited with Ni/Au (50/50 nm) followed by lift-off process. Fig. 1(b) shows the scanning electron microscopy (SEM) image of the fabricated fin-MOSHEMT with fin width of 210 nm. The trench at the gate area shows the recessed Al_2O_3 from 33 nm to 5 nm. A small 3% lattice mismatch exhibits between MgCaO and barrier layer, determined by X-ray diffraction (XRD) experiment. Fig. 1(c) is a high-resolution TEM image of oxide/fin structures after oxide deposition. MgCaO (111) can be epitaxially grown on AlGaN (0001) surface with wurtzite structure [17]. Single crystalline MgCaO on the fin top provides a high quality interface for channel control. The lithography processes were performed by a Vistec VB6 e-beam lithography system and a MJB3 Kurss Mask Aligner. The DC and pulse measurements were carried out with Keithley 4200 Semiconductor Characterization System and Keysight B1530A at room temperature. The off-state breakdown measurements were performed using Agilent B1505A high-voltage semiconductor analyzer system.

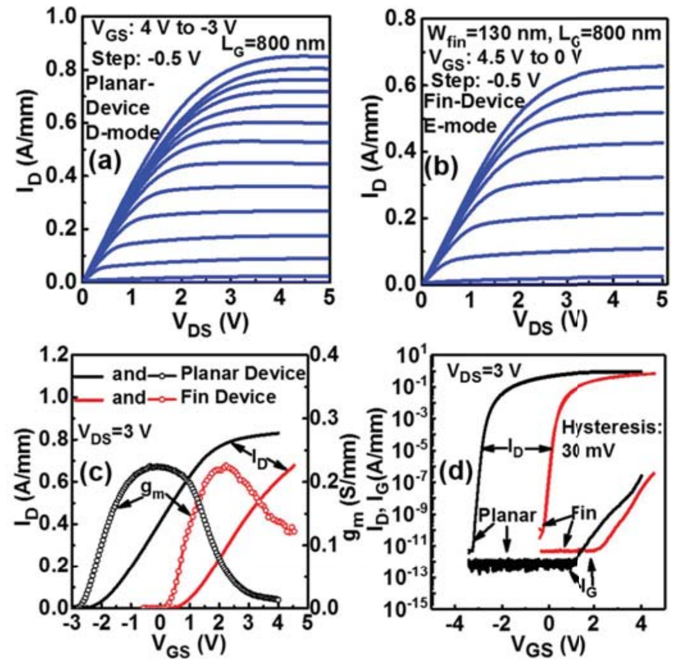

Fig. 2. (a) I_D-V_{DS} of a planar GaN MOSHEMT with L_G = 800 nm and L_{SD} = 4.5 μm. (b) I_D-V_{DS} of a GaN fin-MOSHEMT with L_G = 800 nm, L_{SD} = 4.5 μm, and W_{fin} = 130 nm. (c) and (d) are linear-scale I_D-g_m-V_{GS} and I_D-V_{GS} hysteresis with low I_G of planar and fin MOSHEMTs, respectively. E-mode fin MOSHEMT is with V_T = 1 V, high on/off ratio of 10^{11} and negligible hysteresis of 30 mV.

III. Results and Discussion

Fig. 2(a) shows the well-behaved DC output characteristics (I_D-V_{DS}) of a planar MOSHEMT with L_G = 800 nm and L_{SD} = 4.5 μm. The V_{DS} is swept from 0 to 5 V and the V_{GS} is stepped from 4 V to −3 V with −0.5 V as a step. I_{DMAX} of 0.85 A/mm is realized for the planar MOSHEMTs. Fig. 2(b) shows the similar DC I_D-V_{DS} of a fin-MOSHEMT with the same L_G and L_{SD} and a W_{fin} = 130 nm. The V_{DS} is swept from 0 to 5 V and the V_{GS} is stepped from 4.5 V to 0 V with −0.5 V as a step. I_{DMAX} is 0.67 A/mm for the fin-MOSHEMTs.

The gate width of planar and fin MOSHEMTs are 10 μm and 3.25 μm, respectively. The I_D of fin-MOSHEMT is normalized with the fin width, since the device area without AlGaN barrier on the sidewalls delivers no current and the negative charges at the fin sidewall/oxide interface also prevent electron accumulation and conduction on the sidewalls. An on-resistance (R_{on}) of 3.4 $\Omega \cdot$ mm has been achieved on the fin-MOSHEMT. The linear-scale I_D-g_m-V_{GS} and log-scale I_D-V_{GS} hysteresis with low I_G of GaN MOSHEMTs are plotted in Fig. 2(c) and 2(d), respectively. The V_T of planar and fin-MOSHEMTs are extracted to be −2 and 1 V, which are determined by the linear extrapolation of I_D-V_{GS} at V_{DS} = 3 V. The net negative charge density (n) introduced by the MgCaO on fin-MOSHEMTs is roughly estimated to be 4.9×10^{12} cm^{-2} by using n = C$\cdot\Delta V_T$/q, where C and

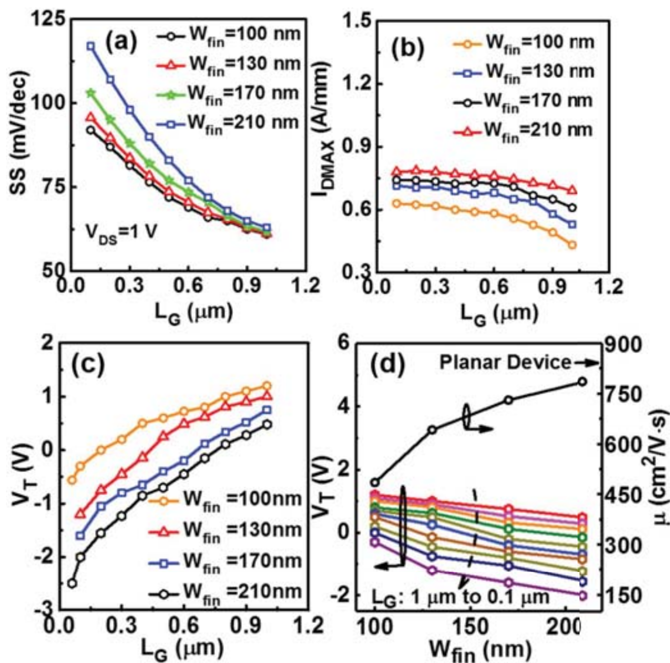

Fig. 3. (a) SS and (b) I_{DMAX} scaling metrics of fin-MOSHEMTs with various fin width from 100 nm to 210 nm. (c) V_T scaling metrics with W_{fin} from 100 nm to 210 nm and (d) Fin width dependent electron mobility and V_T scaling metrics with L_G from 100 nm to 1 μm.

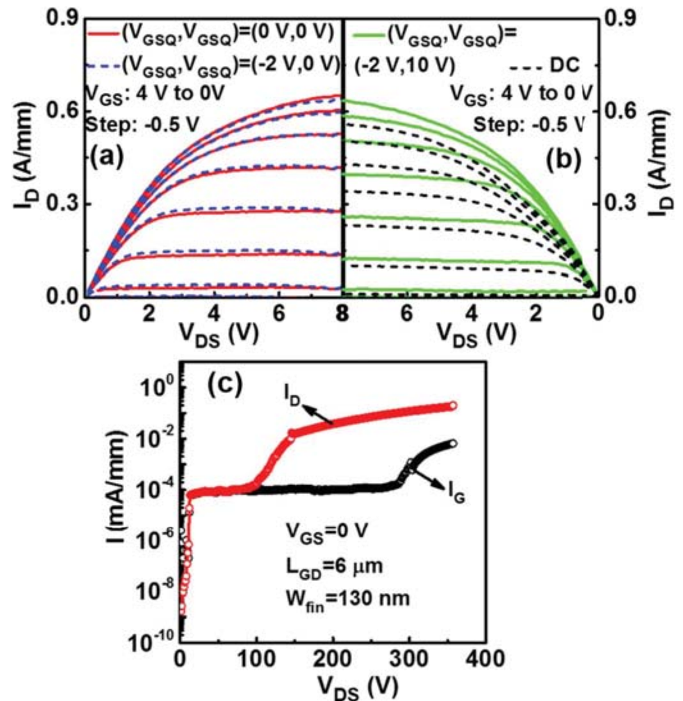

Fig. 4. (a) and (b) are pulse measurements of a fin-MOSHEMT with $W_{fin}/L_G/L_{GD}$ = 0.13/1/12 μm and pulse width/period = 0.5 μs/1 ms, respectively. (c) Three-terminal off-state breakdown measurement with L_G/L_{GD} = 1/6 μm and W_{fin} = 130 nm.

ΔV_T are gate capacitance, V_T difference and electron charge quantity, respectively. The extrinsic peak transconductances (g_{max}) are calculated to be 0.23 and 0.22 S/mm for planar and fin-MOSHEMT, respectively. The log-scale transfer characteristics of I_D-V_{GS} clearly show a high on/off ratio of $10^{11} \sim 10^{12}$ and $10^{10} \sim 10^{11}$ for planar and fin MOSHEMT, respectively. The near one order higher normalized off-state I_D is most likely from smaller effective gate width of fin-MOSHEMT and current leakage paths from side walls of fin structures. Near ideal (~64 mV/dec) substhreshold slope (SS) of both devices are achieved, showing the superior gate control capability of the MOSHEMT with epitaxy oxide. The hysteresis is just 30 mV when the V_{GS} is first swept from negative to positive and then swept back, further confirming the MgCaO/AlGaN interfaces both on barrier top and fin sidewalls are of high-quality. The gate leakage current (I_G) is only 0.3 μA/mm at V_{GS} = 4.5 V. Fig. 3(a) and 3(b) are SS and I_{DMAX} scaling metrics of fin-MOSHEMTs with various fin width from 100 nm to 210 nm, respectively. By increasing the fin width the I_{DMAX} is increased, showing the electron mobility is increased. Fig. 3(c) is the V_T scaling metrics of the fin-MOSHEMTs with various W_{fin}. The smaller W_{fin} is, the more positive V_T is. Standard V_T roll-off behavior is observed when the L_G is reduced from 1 μm to 100 nm. The short channel effect is also mitigated with less severe V_T roll-off when the W_{fin} is reduced. Fig. 3(d) describes fin width dependent electron mobility μ and V_T scaling metrics with L_G from 100 nm to 1 μm. The μ of fin-MOSHEMTs with W_{fin} = 100, 130, 170, and 210 nm and planar MOSHEMT are 485, 642, 731, 786, and 840 cm^2/V·s at L_G = 1 μm and V_{GS}-V_T = 3.5 V, respectively. Increased μ of wider fin structures confirms the degradation of μ by the side-walls in narrow fin structures.

Fig. 4(a) and 4(b) depicts the pulse measurements of a long gate to drain spacing (L_{GD}) fin MOSHEMT to study the passivation effect of the MgCaO oxide. The pulse width and period are 500 ns and 1 ms, and the quiescent bias points are set at (V_{GSQ}, V_{DSQ}) = (0 V, 0 V), (−2 V, 0 V), and (−2 V, 10 V) for cold channel, gate and drain pulses, respectively. Compared with (0 V, 0 V) pulsed saturation current, both the gate and drain pulsed saturation currents show negligible current collapse. All of the pulsed saturation currents are higher than the DC current, showing the good passivation effect of the MgCaO as a dielectric for power device. The three-terminal off-state breakdown measurement is shown in Fig. 4(c). The device is with W_{fin} = 130 nm, L_G = 1 μm, and L_{GD} = 6 μm. Both the source and gate are grounded when the V_{DS} is slowly increased and until the off-state I_D reaches 1 mA/mm. A breakdown voltage (BV) of 365 V is achieved at I_D = 0.2 mA/mm. Further increasing the L_{GD} shows no significant improvement in increasing the BV, which is limited by the 600 nm buffer thickness. Optimization of the device structure by increasing the buffer thickness is expected to improve the BV.

IV. Conclusion

We have experimentally demonstrated a new approach to realize high performance E-mode GaN MOSHEMT with V_T = 1 V through dielectric charge engineering. Taking advantage of its high I_{DMAX} of 670 mA/mm, high on/off ratio of $10^{10} \sim 10^{12}$, low I_D-V_{GS} hysteresis of 30 mV, and negligible current collapse, GaN fin-MOSHEMTs show their great promise for the future power electronics applications.

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